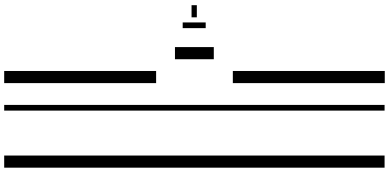


Radiation Hardness of Digital Pixel Sensor Prototypes in 65 nm CMOS Technology for the ALICE ITS3 Upgrade

Master Thesis

Nicolas Tiltmann

Westfälische Wilhelms-Universität Münster
Institut für Kernphysik
AG Andronic / Klein-Bösing

First Referee: Prof. Dr. Anton Andronic
Second Referee: Prof. Dr. Christian Klein-Bösing

Münster, September 2023

Abstract

The ALICE Inner Tracking System will be upgraded to its third version (ITS3) in the LHC Long Shutdown 3 (2026-2028). The ITS Inner Barrel will be replaced by a truly cylindrical detector consisting of six half-layers from stitched wafer-scale monolithic active pixel sensors (MAPS). The sensor chip will produced in the *TPSCo.* 65 nm CMOS technology. In a first submission in this technology, several different test structures were produced. One of them is the Digital Pixel Test Structure (DPTS), which features 1024 pixel with a digital readout.

In order to evaluate the radiation hardness of this test structure, irradiation campaigns with X-rays as well as with neutrons were carried out. Results from these studies demonstrate sufficient radiation hardness of these structures to ionizing doses of 10 kGy and non-ionizing doses of 10^{13} 1 MeV n_{eq} cm^{-2} as required for the ITS3. Moreover, this technology is candidate for the potentially upcoming ALICE 3 upgrade, where much higher radiation doses are expected. First results indicate that a sufficient ionizing radiation hardness is realistic in this technology. The non-ionizing radiation hardness is not sufficiently demonstrated yet. However, previous studies focused mainly on the operation at room temperature whereas sub-zero cooling is a viable option for ALICE 3.

Contents

1 Introduction **1**

2 The Standard Model and the Quark-Gluon Plasma **2**

2.1 The Strong Interaction 3

2.2 Quark-Gluon Plasma 4

3 Semiconductor Detectors **6**

3.1 Basics of Semiconductors 6

3.2 Particle Interaction and Signal Generation 9

3.3 Radiation Effects in Semiconductor Detectors 11

3.3.1 TID Damage 11

3.3.2 NIEL Damage 12

3.4 Segmented Semiconductors 13

3.5 Applications in High-Energy Physics Tracking Systems 13

3.6 Generation of X-rays with ^{55}Fe 15

4 LHC, ALICE and the ITS3 Upgrade **17**

4.1 Large Hadron Collider 17

4.2 ALICE 18

4.3 The ALICE Inner Tracking System 19

4.3.1 ITS 19

4.3.2 ITS2 20

4.3.3 ITS3 22

5 The MLR1 Test System **25**

5.1 Digital Pixel Test Structure (DPTS) 25

5.2 Test System 32

6 Experimental Setup **34**

6.1 Data Compression 35

6.2 Shift Register Test 36

6.3 Monitor Pixel . . . 37
6.4 Fake-Hit Rate Scan . . . 37
6.5 Threshold Scan . . . 39
6.6 Decoding Calibration . . . 40
6.7 ^{55}Fe Source Scan . . . 42
6.8 Beam Test Setup and Analysis . . . 45

7 Ionizing Radiation 47
7.1 Setup . . . 47
7.2 Chip Current Measurements . . . 49
7.3 Threshold . . . 53
7.3.1 Constant Biasing Parameters . . . 54
7.3.2 Tuning for Constant Threshold . . . 55
7.4 Fake-Hit Rate . . . 58
7.4.1 Constant Biasing Parameters . . . 58
7.4.2 Tuning for Constant Threshold . . . 61
7.5 Studies on Sensors with Higher X-Ray Doses . . . 62
7.6 Annealing . . . 63
7.7 Energy Calibration . . . 69
7.8 Efficiency . . . 72
7.9 Summary . . . 74

8 Non-Ionizing Radiation 76
8.1 Setup . . . 76
8.2 Temperature Dependency . . . 77
8.2.1 Constant Biasing Parameters . . . 77
8.2.2 Tuning for Constant Threshold . . . 80
8.3 Energy Calibration . . . 84
8.4 Efficiency . . . 85
8.5 Studies on Sensors with Higher Neutron Doses . . . 87
8.6 Summary . . . 90

9 Conclusion and Outlook 92

A Additional Details on the Beam Test Setup 94

B Measurement of S-Curve Noise 98

C Additional Plots **102**

C.1 Ionizing Radiation 102

C.2 Non-Ionizing Radiation 113

Bibliography **115**

Declaration **118**

Acknowledgements **119**

List of Acronyms

ADC	Analog-Digital Converter
ALICE	A Large Ion Collider Experiment
ALPIDE	ALICE Pixel Detector
APTS	Analogue Pixel Test Structure
BoB	Breakout Board
CML	Current-Mode Logic
CMOS	Complementary Metal-Oxide-Semiconductor
DAC	Digital-Analog Converter
DAQ	Data Acquisition
DPTS	Digital Pixel Test Structure
DUT	Device under Test
FET	Field-Effect Transistor
FHR	Fake-Hit Rate
FPC	Flexible Printed Circuit
FPGA	Field Programmable Gate Array
IB	Inner Barrel
IP	Interaction Point
ITS	Inner Tracking System
LHC	Large Hadron Collider
LoI	Letter of Intent
MAPS	Monolithic Active Pixel Sensor
MIP	Minimum Ionizing Particle
NIEL	Non-Ionizing Energy Loss
NMOS	N-Type Metal-Oxide-Semiconductor
OB	Outer Barrel
PCB	Printed Circuit Board
PID	Particle Identification
PMOS	P-Type Metal-Oxide-Semiconductor
PS	Proton Synchrotron
RHIC	Relativistic Heavy Ion Collider
SDD	Silicon Drift Detector
SPD	Silicon Pixel Detector
SPS	Super Proton Synchrotron
SSD	Silicon Strip Detector
TDR	Technical Design Report
TID	Total Ionizing Dose
ToT	Time-over-Threshold
TPC	Time-Projection Chamber
QGP	Quark-Gluon Plasma

1 Introduction

The ALICE (A Large Ion Collider Experiment) experiment at CERN is dedicated to the study of ultrarelativistic heavy-ion collisions. This is done to deepen knowledge about the Quark-Gluon Plasma (QGP), a state of matter, in which quarks and gluons can exist as free particles. As the QGP exists for only fractions of a second, only particles emerging from that QGP can be detected and used as a probe for the QGP. To cover a large variety of different probes, the ALICE experiment hosts many different subdetectors optimized for different measurements. The innermost detector, Inner Tracking System (ITS), is a silicon-based detector. It is used to measure the tracks of particles created in the collision precisely in the first section after the interaction point. The tracking continued by the gas-based Time Projection Chamber (TPC), which features a lower spatial resolution, but covers a much larger volume.

A low spatial resolution of the ITS is crucial in order to be able to precisely determine the origin of a track, i.e. the point in space, where a certain particle was produced. In the LHC Long Shutdown 2 (LS2), the ITS was entirely replaced by the ITS2, which is a detector made up of 7 layers of monolithic active pixel sensors. During LHC Long Shutdown 3 (LS3), the innermost 3 layers will again be replaced by a new detector system made of 6 stitched wafer-scale half-layers, with close to no material in addition apart from the wafer itself. This will heavily reduce the material budget and thus increase the track impact parameter resolution.

During the runtime of the detector, the sensors will be exposed to various types of particle radiation, which can potentially damage the detector and degrade its performance. In an R&D effort for the ITS3, several pixel test structures where produced. The Digital Pixel Test Structure (DPTS) hosts 1024 pixel. In this thesis, several aspects of the radiation hardness of the DPTS are studied. This includes damages from ionizing radiation as well as non-ionizing radiation. The ionizing radiation hardness is tested with X-rays and the non-ionizing radiation hardness with neutrons.

Lastly, the ALICE experiment is envisaged to be upgraded to a whole new detector, called ALICE 3. The ALICE 3 Vertex Detector will take over the functionality of the ITS. During its runtime, much higher radiation doses are expected. In order to scope possible technologies, all results can also be evaluated with those increased particle loads.

2 The Standard Model and the Quark-Gluon Plasma

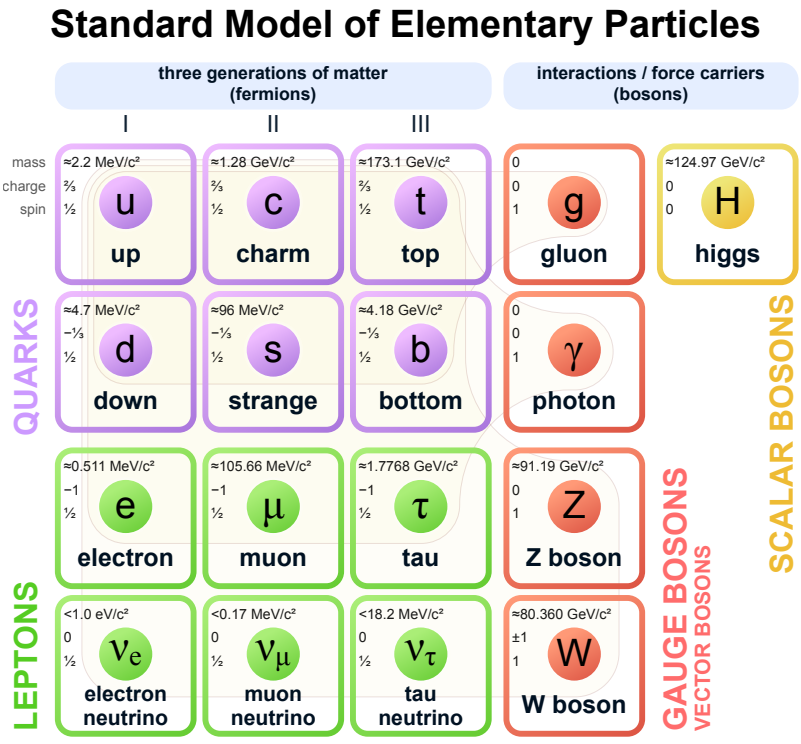
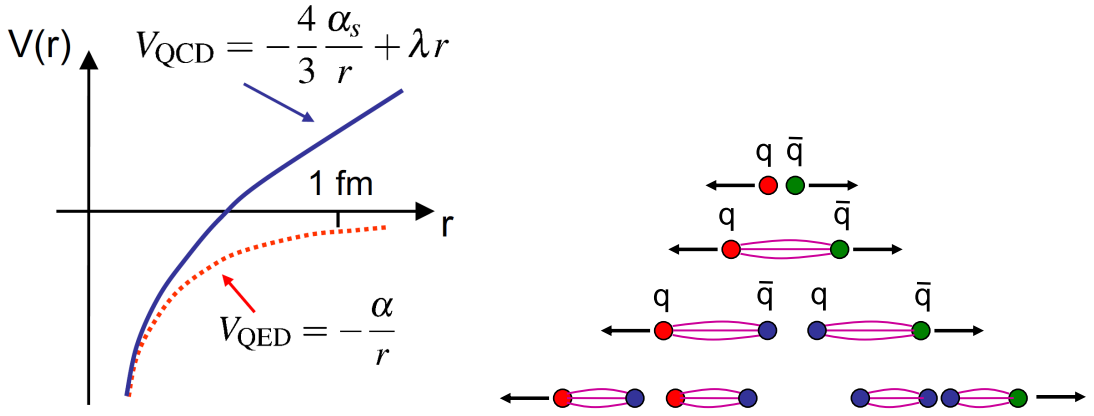


Figure 2.1: Particles in the Standard Model of particle physics. Taken from [Mis19].

The Standard Model of particle physics is an approach to describe all interactions of all known particles. Despite having known weaknesses, it is exceptionally successful in describing the nature of particles. The Standard Model includes a total of 17 fundamental particles. These can be divided into 6 quarks, 6 leptons and 5 interaction particles. An overview of the particles described in the Standard Model is given in figure 2.1. Quarks are massive particles having an electric and a so-called color charge. Therefore, they are participating in processes of all fundamental forces: strong, weak, and electromagnetic interaction. The quarks are named up (u), down (d), strange (s), charm (c), bottom (b) and top (t), sorted in order of increasing mass. The class of leptons contains three massive particles: the electron (e), the

muon (μ), and the tau (τ), also sorted in order of increasing mass. In contrast to the quarks, leptons do not carry a color charge and because of this, they do not participate in the strong interaction. They do, however, interact via the electromagnetic and weak interaction. The other three leptons are called neutrinos. In analogy to the massive leptons, they are called electron neutrino ν_e, muon neutrino ν_μ and tau neutrino ν_τ. These particles do not carry an electric charge. Therefore, they only interact via the weak interaction. Within the Standard Model, neutrinos are massless. However, more recent measurements indicate that neutrinos are in fact not massless, which is not accounted for in the Standard Model. The class of interaction particles contains the gluon (g), the photon (γ) and the Z and the W bosons, which are the force carriers of the strong, electromagnetic and weak interaction respectively. The Higgs boson (H) was experimentally found by the ATLAS and CMS experiment at CERN in 2012. The Higgs boson couples to elementary particles with a strength proportional to the particle mass, effectively being responsible for giving mass to them. In addition to every particle, there exists an antiparticle. In an antiparticle, all charge-like quantum numbers, such as the electric charge and the color charge are inverted. All other properties are the same with respect to its particle. The fourth fundamental force, gravitation, is not described by the Standard Model. On small scales, gravitation can be neglected because on the scale of fundamental particles, it is 33 orders of magnitude weaker than the weak interaction. [Dem17]

2.1 The Strong Interaction



(a) QCD and QED potential (b) String breaking

Figure 2.2: (a) Potentials of strong interaction described by Quantum Chromodynamics (QCD) and electromagnetic interaction described by Quantum Electrodynamics (QED) (b) String breaking in mesons and the resulting confinement. Both taken from [Tho09].

The strong interaction is described by a quantum field theory called Quantum Chromodynamics (QCD). Particles that carry a color charge are affected by the strong interaction. There are three colors blue, red, and green and three respective anticolors, anti-blue, anti-red, and anti-green. The strong interaction is mediated by gluons. In contrast to photons in the electromagnetic interaction, gluon themselves carry charges, in detail one color and one anticolor. This is emerging from the underlying SU(3) symmetry group that is the basis of QCD. [Dem17] The potential of QCD can be written as [Tho09]

$$V_{\mathrm{QCD}} = -\frac{4}{3}\frac{\alpha_{\mathrm{s}}}{r} + \lambda r, \tag{2.1}$$

where α_{s} is the coupling constant of the strong interaction and r the distance for color charged particles. λ is the string tension, which is usually given with a value of about $1\,\mathrm{GeV\,fm^{-1}}$ [And+83]. Figure 2.2a shows a sketch of the QCD potential compared to the well-known potential of two electric charges as it can be derived from Quantum Electrodynamics (QED). For short distances r, both potentials follow the same $1/r$ behavior. However at long distances, the QED potential asymptotically approaches 0, while the QCD potential rises linearly. Consequently, the energy stored in the bond between two color charges rises indefinitely with increasing distance r. At some point, this energy will surpass the energy needed to create a quark-antiquark pair, which is what then happens. This is sketched in figure 2.2b. Because of this, no color charges can be observed freely. Generally, either a color and its respective anticolor combine to a net-zero color charge, as it is observed in mesons, or all three colors (r, g, b) combine to a net-zero color charge, as it is seen in baryons as for example protons. This holds true for all known particle systems. This phenomenon is called color confinement. Going to very small distances, the opposite is observed. The coupling constant α_{S} is becoming smaller with decreasing distance. On a small scale, quarks can be treated as free particles. [Dem17]

2.2 Quark-Gluon Plasma

Due to the color confinement, in regular matter, color charges cannot be observed freely. There is, however, a state of matter where quarks and gluons can move freely. In analogy to a plasma, where ions and electrons can move freely, this state is called Quark-Gluon Plasma. In order to bring matter into such a state, extreme temperatures and baryon densities are needed. The Quark-Gluon Plasma can, on earth, only be produced in high-energy heavy-ion collisions. In fixed-target experiments, due to special relativity, the maximum collision energy is rather limited. On the other hand, very high particle densities can be reached. In colliding-beam experiments, the collision energy can be much higher, although at the cost of

decreased particle densities. In both cases, high energy and density can be only sustained for a very short amount of time, so that the Quark-Gluon Plasma can be only observed indirectly through certain phenomena that emerge from its nature. First experimental evidence for the existence has been collected at the CERN SPS in 2000. Measurements were refined by the BNL RHIC and CERN LHC in the following years. [And+18; Col22b]

3 Semiconductor Detectors

Semiconductor detectors are a type of particle detectors. The detection medium is a semiconductor in solid state. Commonly used semiconductors are silicon (Si), germanium (Ge) or gallium arsenide (GaAs) [Spi05]. Positions resolutions in the micrometer scale can be achieved with silicon-based detectors. The following chapter will focus on silicon as detection medium only.

The operation of a semiconductor detector requires certain buildings blocks, which are the active medium itself, signal shaping and amplification, signal processing as well as a analog-to-digital converter. [Spi05] The exact realization of these building blocks can vary widely. The availability of CMOS circuits in silicon allows signal processing to be integrated in the same device as the active medium. In this way, monolithic active pixel sensors (MAPS) can be produced.

In the active medium of a semiconductor detector, impinging particles create free charge carriers by ionization. Electrons and holes can immediately recombine or diffuse through the active medium. As free charge carriers move in the active medium, an electric current can be measured at the collection electrodes. Under presence of an electric field, electrons and hole can also drift. As this increases the charge collection speed, it reduces the probability for recombination of electrons and holes. Recombined charge carriers do not contribute to the signal. The principle of signal generation and collection is shown in figure 3.1. Finally, the generated charge is proportional to the energy deposited in the active medium. [Spi05] An overview about different theoretical aspects of semiconductors is given in the following sections. It is shown, how an internal electric field in the detector can be created by a pn-junction, removing the need for an external field.

3.1 Basics of Semiconductors

Semiconductors are elements with an electrical conductivity between conductors and insulators. Their band gap is smaller than the band gap of insulators, but larger than the band gap of metals. Silicon is a semiconductor from the fourth group of the periodic table. Its bandgap is $E_g = 1.12\,\mathrm{eV}$ [Spi05]. Within the crystal, every silicon atom has bonds to four

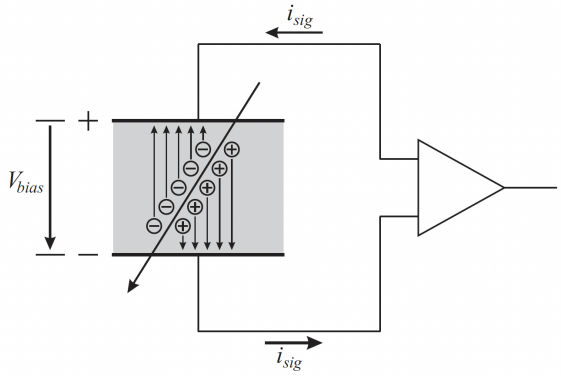


Figure 3.1: Example of charge collection within in an ionization chamber. This ionization chamber could for example be a semiconductor like silicon. Taken from [Spi05, Fig. 1.9, P. 9].

neighboring atoms. Impurities in the crystal lattice can alter its electrical properties. Doping makes use of this effect. Implanting atoms from the third group creates holes in the crystal lattice, which can act as acceptors. Little energy is needed to move an electron from another atom into this hole effectively moving the hole to another lattice site. For silicon as bulk material, often Boron (B) is used. The resulting material is called "p-type". By implanting atoms from the fifth group, donators are introduced, as the additional electron is not strongly bound. Phosphorous (P) is frequently used and the result is a "n-type" semiconductor. As mentioned, the dopant atoms can change the properties of the crystal lattice. The presence of lightly bound charge carriers increases the conductivity. [Spi05] The concentration of doping atoms can vary strongly. Subscripts are often used to stress different doping levels in different parts of a semiconductor system. For example, P^+ silicon is more heavily doped with holes than $P^=$.

If a p- and a n-type regions are brought into contact with each other, electrons and holes diffuse over all of the crystal. As electrons diffuse away from the n-type region, they leave positively charged holes in the crystal lattice. The opposite is happening for holes, as electron-filled hole sites are negatively charged. An electric field between the n-type region and p-type region is built, counteracting the charge carrier moving until an equilibrium is reached. This is visualized in figure 3.2. The zone is referred to as the depletion region, as there are no free charge carriers present. Alternatively, it is described as space charge region as this region is the only part of the crystal showing a macroscopic electric field. The absence of free charge carriers makes the pn-junction an insulator if no external field is present. [Spi05]

By applying an external field, the size of the depletion region can be varied. A *reverse bias* is applied if the negative terminal of the voltage source is connected to the p-type region and vice versa. The increase availability of electrons in the p-type will fill holes and therefore

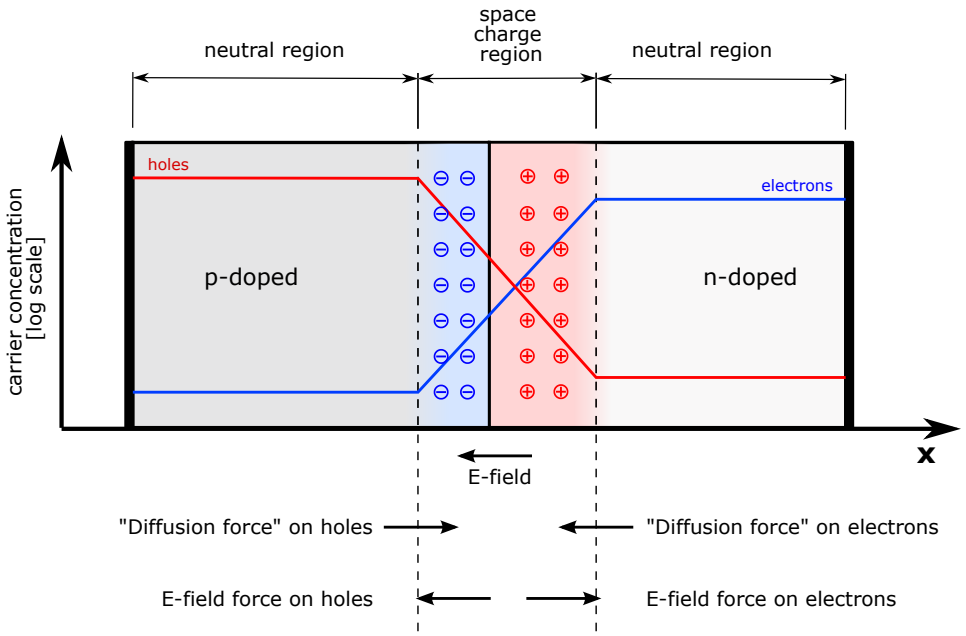


Figure 3.2: Schematic drawing of a pn-junction. Taken from [The07], background removed.

increasing the depletion region. In the n-type region, additional electrons will leave the crystal, increasing the depletion region also on that side. [Spi05] The depletion region is important for semiconductor detectors, as the presence of an electric field enables effective separation of electron-hole pairs generated by particles crossing the detector. The drift of the charge carriers is then creating an electric signal at the electrodes.

At room temperature, the depletion region is not an ideal insulator. Thermally excited electrons are still able to cross the depletion region. Thus, even without ionization from e.g. an incident particle, a small current will flow. This is called leakage current. The leakage current strongly depends on the level of impurities in the crystal lattice. With impurities present, electrons do not have to traverse the whole depletion region at once. Furthermore, the temperature exponentially influences the leakage current, which follows [Spi05, Eq. (1.13), P. 16]

$$I_{\text{leakage}} \propto T^2 \exp\left(-\frac{E_g}{2k_{\text{B}}T}\right). \tag{3.1}$$

T is the temperature, k_{B} Boltzmann's constant and E_g the band gap of silicon of 1.12 eV. In general, leakage current is unwanted, as it increases the power consumption as well as the noise. A good approach to limit the leakage current is to control the temperature of the sensor, as a decrease of 14 °C will cut the leakage current by a factor of 10 [Spi05].

3.2 Particle Interaction and Signal Generation

As discussed before, impinging particles create free charge carriers in a semiconductor. In this section, more details are given on how the interaction of incident particles with the semiconductor works. Furthermore, it is discussed, how an electric signal is emerging from these effects.

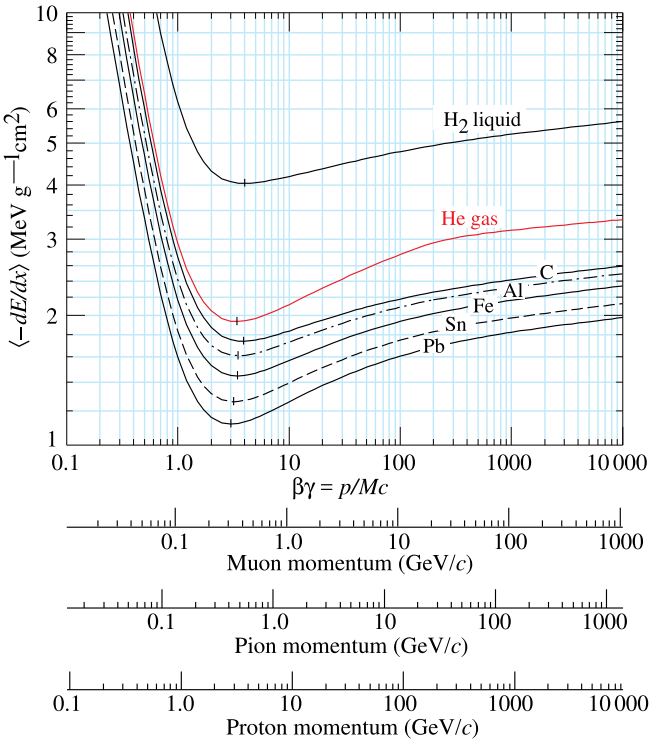


Figure 3.3: Exemplary mean energy loss curves for different incident particles and different target materials. Taken from [Wor+22].

Charged and massive particles, such as protons loose, parts of their energy, when traversing through matter. The energy loss per distance $\frac{\mathrm{d}E}{\mathrm{d}x}$ is dependent of the particle species and its energy and can be described by the Bethe-Bloch formula [Wor+22]:

$$\left\langle -\frac{\mathrm{d}E}{\mathrm{d}x} \right\rangle = 4\pi N_A r_\mathrm{e} m_\mathrm{e} c^2 z^2 \frac{Z}{A} \frac{1}{\beta^2} \left[\frac{1}{2} \ln \frac{2 m_\mathrm{e} c^2 \beta^2 \gamma^2 W_\mathrm{max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2} \right] \tag{3.2}$$

This formula is valid for charged particles with $0.1 \leq \beta\gamma \leq 1000$ [Wor+22]. Moreover, the formula is not suited to describe electrons as projectiles, as additional interaction processes have to be considered there. z is the charge number of the incident particle and Z the charge number of the absorber. A is the mass number of the absorber, N_A Avogadro's constant, $r_\mathrm{e} = e^2/4\pi\epsilon_0 m_\mathrm{e} c^2$ the classic electron radius, m_e the electron mass, c the speed of light, $\beta = \frac{v}{c}$, $\gamma = 1/\sqrt{1 - v^2/c^2}$, W_max the maximum possible energy transfer in a single collision and I the mean excitation energy in eV. The term $\delta(\beta\gamma)/2$ is a density effect correction. At low

particle momenta ($0.1 \leq \beta\gamma \leq 1$), most of the the energy loss is dominated by ionization of the target material. The energy loss decreases with $1/\beta^2$ as the particle momentum increases. At $\beta\gamma \approx 3-4$, the energy loss is minimal. Particles in this regime are called minimum-ionizing particles (MIP). At even higher momenta, the energy loss increases again due to radiative effects. [Wor+22; Dem17] Exemplary mean energy loss curves are shown in figure 3.3. The characteristic minimum for MIPs can be seen for different target materials.

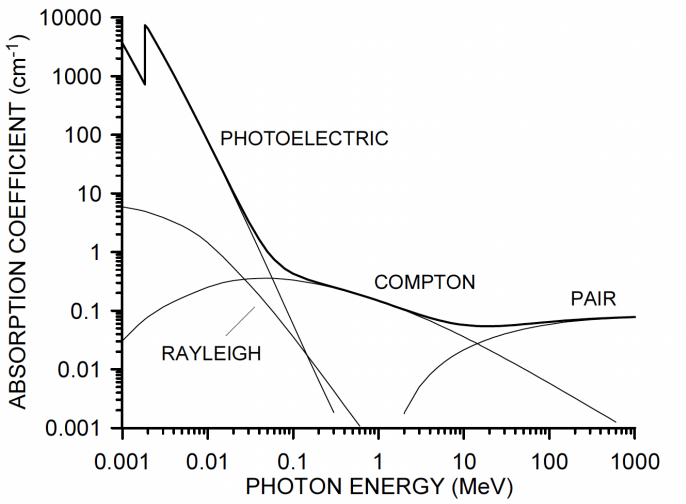


Figure 3.4: Photon absorption coefficient for different energies in silicon. Taken from [Spi05, Fig. 1.20, P. 23].

Photons interact differently with matter. The absorption coefficient for photons in silicon is shown in figure 3.4. At energies below approximately 100 keV, the photo-effect dominates. This is the relevant process for the absorption of X-ray photons from ^{55}Fe discussed in the later chapters. In the photo-effect, a shell electron of the target material is being kicked out of the atom by an impinging photon. The energy of the electron is equal to the energy of the previous photon[1]. Electrons with an energy of ≈ 6 keV have a range in the order of µm and are thus likely being stopped within the active layer. The electron ionizes silicon in the crystal analogously to external incident particles.

The average generated charge in the active medium can be calculated as [Spi05, Eq. (1.5), P. 12]

$$Q_s = \frac{E}{E_i} e, \tag{3.3}$$

where E is the energy deposited in the active medium by the traversing particle. E_i is the average energy to create an electron-hole pair in silicon and e is the elementary charge. E_i is

[1] A small portion of the energy is needed for the ionization. At photon energies of 6 keV, this is negligible.

approximately 3.6 eV for silicon. The band gap of silicon is only about 1/3 of this value. Due to energy and momentum conservation, a large portion of the energy goes into excitation of the lattice. [Spi05] In combination with the capacitance of the sensor C_{sensor} a voltage

$$V_{\text{signal}} = \frac{Q_s}{C_{\text{sensor}}} \tag{3.4}$$

can be measured.

3.3 Radiation Effects in Semiconductor Detectors

Per definition, particle detectors are constantly subject to irradiation. Several effects will impact the sensor performance. For semiconductor detectors, there are two major mechanisms of radiation damage, which are discussed in detail in the following.

3.3.1 TID Damage

On top of the epitaxial layer, a layer of silicon dioxide (SiO_2) is placed in order to achieve electrical isolation between the silicon and the metal layers of the MOS. TID damages are mainly generating surface defects, which are affecting the region of the circuitry in the sensor. An energy of about 18 eV is needed, to create an electron-hole pair in the SiO_2 oxide layer. Ionization in this layer also creates an electron-hole pair. On the one hand, the electron has high mobility and is able to leave the layer. On the other hand, the movement process of the hole in this layer is very complex. Holes can be trapped at certain positions in the oxide layer. The presence of a hole at the oxide-silicon boundary means an additional positive charge, which lastly alters the electric field. This can potentially change the characteristics of the transistor and therefore of the whole frond-end circuit. [Spi05]

The effects introduced by ionizing radiation are only dependent on the amount of absorbed energy. If the density of the sensor is constant, the ionization damage per volume is proportional to the absorbed energy per mass, which is given in units of $\frac{\text{J}}{\text{kg}} = \text{Gy}$. This energy is also referred to as Total Ionizing Dose (TID). As the ionization energy is material-dependent, the TID has to be given with respect to the material of interest. [Spi05]

Due to presence of thermal activity within the crystal lattice, the mobility of a trapped hole can be increased. If the hole is being untrapped, the previously induced damage is healed. The process is called annealing and is heavily temperature-dependent. Only little annealing occurs at room temperature. At temperatures of more than 100 °C significant annealing could be achieved in a short amount of time. [Spi05; Wer+06]

3.3.2 NIEL Damage

Damage by non-ionizing energy loss is created by the interaction of incident particles with the nuclei of the crystal lattice and can alter the electrical properties of the active medium. In a silicon crystal, an energy of about 25 eV is needed to fully displace a silicon atom from its lattice position. The collision of the incident particles with a lattice atom is restricted by the energy and momentum conservation. Therefore, the actual recoil of the silicon atom depends on the species and energy of the incident particle. For example, a 1 MeV neutron will displace about 1000 silicon atoms in an area with a size in the order of 0.1 µm. [Spi05]

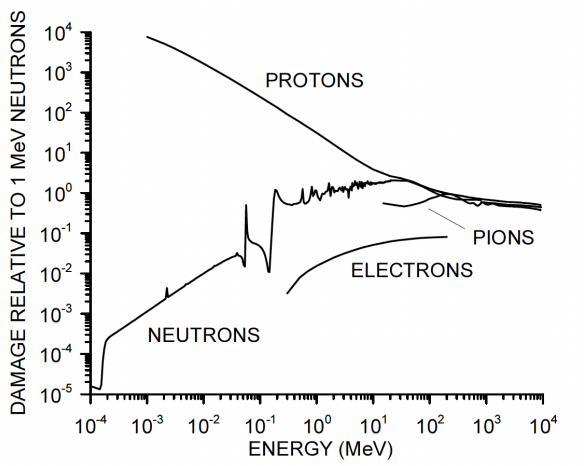


Figure 3.5: Non-ionizing damage vs. energy for different incident particles, plotted relative to 1 MeV neutrons. Taken from [Spi05, Fig. 7.1, P. 280].

Figure 3.5 shows the relative non-ionizing damage of different incident particles with respect to the damage done by neutrons with an energy of 1 MeV. The amount of non-ionizing energy loss (NIEL) is related to the induced damage. It is commonly hypothesized that the non-ionizing energy loss is proportional to the amount of created damage (NIEL-Hypothesis). However, it has been observed experimentally that this hypothesis does not hold true for all particle energies and species. [Spi05] Nevertheless, the non-ionizing energy loss is a useful tool to quantify the damage, especially if only a single particle species, such as neutrons, and a narrow energy range is used. In particular, the non-ionizing dose is given as non-ionizing energy loss relative to 1 MeV neutrons per area, where commonly cm^{-2} is used. This will lead to a unit of dose given as 1 MeV n_{eq} cm^{-2}.

Consequences of NIEL damage are irregularities of the crystal lattice. The three main mechanisms are formation of mid-gap states, creation of states close to the band edges and changing of doping characteristics. Mid-gap states are additional states in the semiconductor which are increasing the probability of movement of electrons through the depletion region. This

increases the leakage current of the sensor (cf. section 3.1). Additional states close to the band edges can temporarily trap charges and therefore alter the characteristics of the semiconductor detector. Lastly, incident particles can cause nuclear reactions of crystal atoms, which can then alter the doping profile. [Spi05]

3.4 Segmented Semiconductors

Position information can be obtained by appropriately segmenting the silicon detector. A one-dimensional position measurement can be realized using silicon strips. The silicon strips of the ALICE ITS Silicon Strip Detector (SSD) (see also section 4.3.1) had a size of $95\,\mu\text{m} \times 4\,\text{cm}$ [Aam+08]. [Spi05]

Silicon Pixel Detectors (SPD) are segmented in two directions by having a full 2d-segmented anode plane on top of the active medium. However, all pads have to be interconnected to the readout. One possibility is to bump bond another microchip for readout with fitting layout on top of this plane. This scheme is widely used (for example in the first version of the ALICE Inner Tracking System, cf. section 4.3.1), but complicated and expensive to produce. [Spi05] The possibility of producing CMOS circuits in silicon enables integration of the readout into the same silicon of the active medium. Such *monolithic* devices can be constructed in different ways. In a Charge Coupled Device (CCD), the charge is temporarily collected in the pixels itself. Another approach is to also integrate amplification circuitry in the pixels. This approach is called *active pixel*. [Spi05]

In monolithic active pixel sensors (MAPS), the active medium and the read-out electronics are produced in the same microelectronic device. The process used for this is very similar to the processes used in the fabrication of optical imaging sensors. A challenge emerging from the high-energy physics application is the expected radiation load. To this date, the radiation hardness of MAPS is limited to approximately 10 kGy and $10^{12}\,1\,\text{MeV}\ \text{n}_{eq}\ \text{cm}^{-2}$. [Wer+06] Therefore, MAPS do not yet offer a full alternative to bump-bonded hybrid pixel systems for applications with very high expected radiation dose, as for example the ATLAS Inner Tracker. In the ALICE Inner Tracking System, where the rate is lower due to less luminosity, a fully MAPS-based detector system was installed in 2022 [Abe+14]. A concrete example of how monolithic active pixel sensors can be realized is given in section 5.1.

3.5 Applications in High-Energy Physics Tracking Systems

Due to the good spatial resolution and the low material budget, silicon detectors are well suited for tracking systems in many high-energy physics experiments, such as at the CERN

LHC. One significant property to consider is the track impact parameter resolution, which represents the minimum distance between a reconstructed particle track and the interaction point. Multiple scattering is among the factors that can limit the maximum achievable track impact parameter resolution. [Wer+06] The scattering angle can be calculated as [Spi05, Eq. (1.3), P. 8]

$$\Theta_{RMS} = \frac{0.0136\,\mathrm{GeV}/c}{p_\mathrm{T}} \sqrt{\frac{x}{X_0}} \left[1 + 0.038 \cdot \ln\left(\frac{x}{X_0}\right)\right], \tag{3.5}$$

where p_T is the transverse momentum of the traversing particle, x the thickness of the detector and X_0 the radiation length. The radiation length is a material-specific constant given in units of length, which describes the length needed to decrease the incident particle energy to $1/e$. To minimize the uncertainty introduced by multiple scattering Θ_{RMS} should be minimized, which can obviously be done by decreasing the material thickness x, when X_0 is fixed by the choice of material, in this case silicon. [Spi05] Additionally, not all of the material will be silicon, as for example electrical connections have to be are implemented using metal layers. The thickness should be minimized, considering mechanical stability, electrical connections, power consumption, and other requirements. In general, one aims at keeping the overall radiation length as small as possible.

Under the assumption that the particle track is reconstructed by two points only, the impact parameter resolution is given by [Spi05, Eq. (1.2), P. 7]

$$\sigma_b^2 \approx \sigma^2 \left[\left(\frac{1}{1 - r_1/r_2}\right)^2 + \left(\frac{1}{r_2/r_1 - 1}\right)^2\right], \tag{3.6}$$

where σ is the spatial resolution of the tracking layers and r_1 and r_2 are the distances of the tracking layers with respect to the interaction point. It can be seen that the track impact parameter resolution profits from a low spatial resolution of the tracking layers as well as from a small ratio r_1/r_2. Thus, the first layer should be as close as possible to the interaction point. These requirements have implications on the pixel design as well as the spatial positioning of the tracking layers in the final detector. [Spi05]

3.6 Generation of X-rays with ^{55}Fe

A widely used source for soft X-rays in lab environments is ^{55}Fe. This isotope decays via electron capture with a probability of 100.00 % [Jun08]. The reaction equation on subatomic level is

$$\mathrm{p} + \mathrm{e}^- \rightarrow \mathrm{n} + \nu_\mathrm{e}. \tag{3.7}$$

As the electrons from the (innermost) K-shell have the probability of being within the the nucleus, it is most likely that an electron from this shell participates in the nuclear reaction. In the moment of reaction, the iron nucleus changed into a manganese nucleus by lowering the charge number by one. The manganese atom is consequently in an excited state as there is a vacancy in the K-shell. This vacancy is filled with an electron from a higher shell as this configuration is energetically more favorable. The excess energy will the be emitted in form of an X-ray photon. As the energy levels of the atom are discrete, only discrete photon energy are emitted. These transitions are then noted as K_α or K_β for filling electrons originating from the L- or M-shell respectively. In case of manganese, these corresponding energies are known as [Jun08]

$$E(\text{Mn-}K_\alpha) = 5.90\,\text{keV} \tag{3.8}$$

$$E(\text{Mn-}K_\beta) = 6.49\,\text{keV}. \tag{3.9}$$

Precisely, these lines are not monoenergetic but the observed lines are composites of, for example, Mn-$K_{\alpha,1}$ and Mn-$K_{\alpha,2}$, which differ by 0.011 keV [Jun08]. This difference in energy cannot be resolved in view of the energy resolution of the detector prototypes used for the work program within this thesis. Physically, these energy differences are a consequence of fine structure effects splitting the energy levels in the atomic shell.

The emission of K_α occurs with a probability of 24.4 % [Jun08], whereas K_β is emitted in 2.9 % [Jun08] of the cases. Thus, the K_α peak is expected to be much more prominent than the K_β peak in recorded spectra. An alternative process is the emission of Auger electrons, where the excess energy is carried away by emission of an outer shell electron. With a probability of 60.1 % [Jun08], an Auger-K electron with an energy of 5.19 keV is emitted. The range of 10 keV electrons is $r_0 = 2.88 \cdot 10^{-4}\,\mathrm{g\,cm^{-2}}$ [Ber+17], while lower energies mean decreased ranges. Combined with the density of air of $\rho = 1.16\,\mathrm{g\,L^{-1}}$ [Wil14] one finds upper limit of the range of $r = \frac{r_0}{\rho} = 2.5\,\mathrm{mm}$, which renders the contribution of Auger electrons towards sensor spectra negligible in this setup. Other possible Auger electrons posses lower energy than the Auger-K and thus their range is even shorter. There are more possible X-ray and

Auger emissions, which add up the probability to 100 %. However, for the spectra, these are negligible, because their relative intensity is quite low and will most likely not be observable as peaks.

The half life of the ^{55}Fe decay is 2.74 years [Jun08] and thus often not negligible when comparing the intensity of ^{55}Fe sources.

4 LHC, ALICE and the ITS3 Upgrade

This chapter provides an overview about the Large Hadron Collider (LHC), the ALICE experiment and in particular the ALICE Inner Tracking System (ITS) and the upcoming ITS3 upgrade.

4.1 Large Hadron Collider

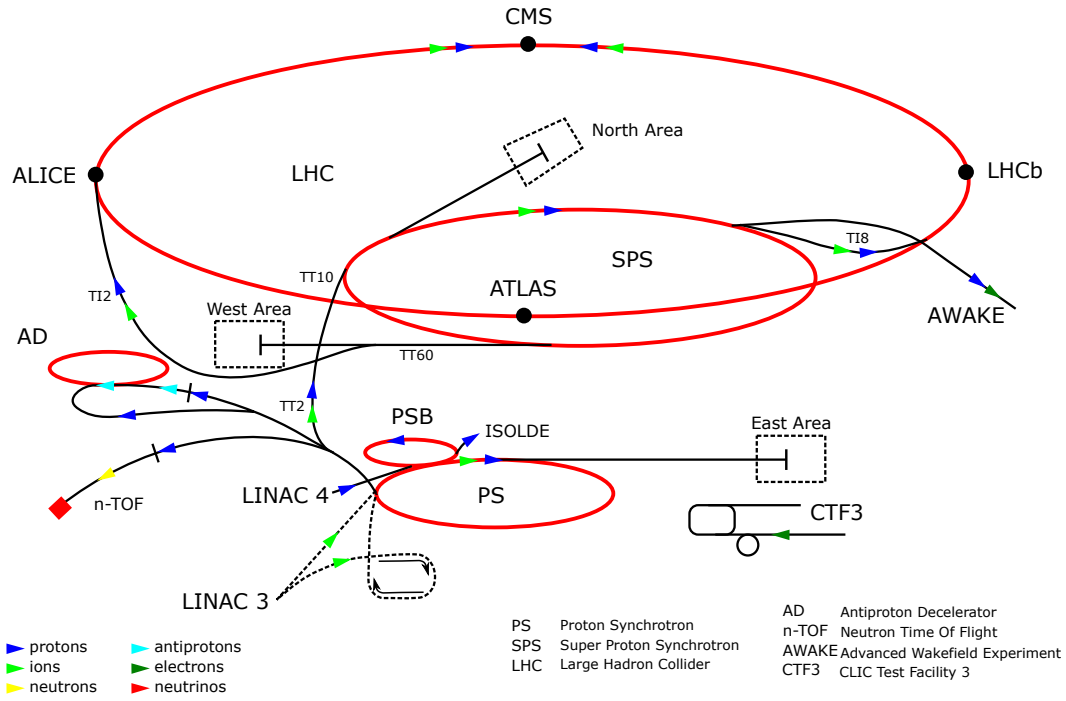


Figure 4.1: Schematic view of the CERN facilities and accelerators. Taken from [For21].

The Large Hadron Collider (LHC) is located at European Organization for Nuclear Research (french: *Organisation européenne pour la recherche nucléaire*, acronym: CERN) across the border between Switzerland and France. To this day, it is the largest particle accelerator for protons and lead-ions. The accelerator was first started up in 2007. A schematic overview of the CERN accelerator complex is given in figure 4.1, where the LHC is the largest red circle. The accelerator itself is a synchrotron located in a approximately 27 km long tunnel. The accelerator is fed with a row of pre-accelerators. For protons, at the time of construction, these

were: Linac 2, PS Booster (PSB), Proton Synchrotron (PS) and Super Proton Synchrotron (SPS). The first is a linear accelerator while the latter ones are synchrotrons. By the start of Run 3 in 2022, Linac 2 has been replaced by Linac 4. During heavy-ion runs, the the initial acceleration takes place in Linac 3. The ions are then further accelerated in the Low Energy Ion Ring (LEIR, not labelled in schematic) after which they are injected into the PS. While being injectors for the LHC, the PS and SPS are also used to deliver hadron beams to fixed-target experiments like CLOUD or NA61/SHINE, as well as freely usable beamlines for prototype tests in the East Area (EA, beam from PS) and North Area (NA, beam from SPS) experimental halls. In the LHC, one beam of hadrons is accelerated clockwise and the other one counterclockwise. At injection, the collision system of two protons has a center-of-mass energy of $\sqrt{s} = 900\,\text{GeV}$. In the LHC, the particles are accelerated up to $\sqrt{s} = 13.6\,\text{TeV}$ for protons and $\sqrt{s_{NN}} = 5.02\,\text{TeV}$ per nucleon pair in lead-lead collisions [Col22b]. There are four points the two beam pipes intersect and hadrons can collide. Around these points four large detectors are installed: ATLAS, ALICE, LHCb and CMS [Col22b].

4.2 ALICE

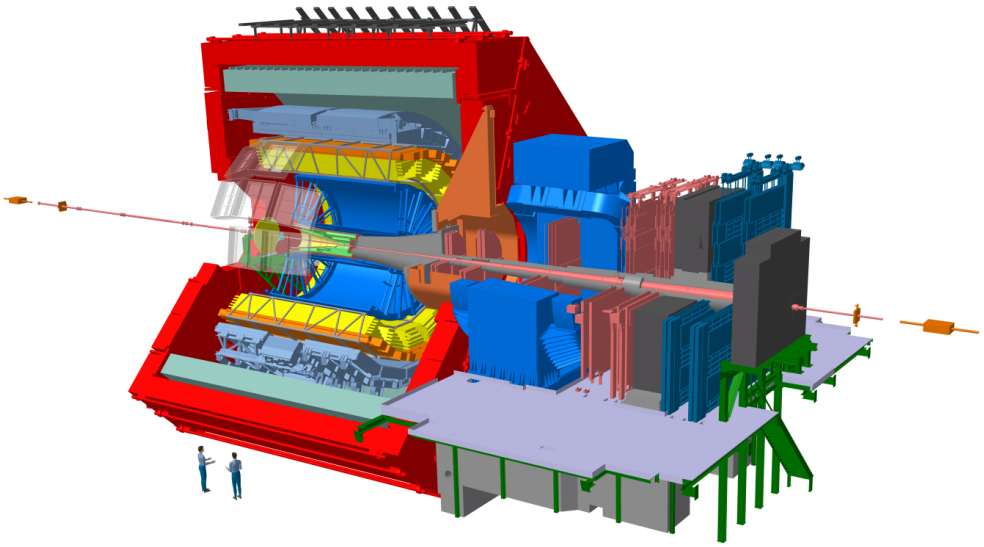


Figure 4.2: Schematic view of the ALICE detector at the start of Run 3. Taken from [Tau17].

The ALICE (A Large Ion Collider Experiment) experiment at CERN is optimized for the study heavy-ion collisions, which is realized as lead-lead in the LHC. In high-energy lead-lead collisions, very high particle densities and temperatures are reached. This creates an environment sufficient for Quark-Gluon Plasma to form. The particles emerging from this short-lived

state of matter can be detected by the ALICE experiment. Despite being optimized for heavy-ion collisions, the ALICE experiment is being used to take data during proton-proton and proton-lead collisions, delivering valuable reference data for the study heavy-ion collisions as well as other dedicated proton-proton collision studies. In figure 4.2, a schematic drawing of the ALICE experiment is given. The detector consists of the central barrel and the muon arm. The central barrel subdetectors are housed within the L3 magnet (red). The magnet is a non-superconducting solenoid creating a static field of up to 0.5 T. The muon arm is installed in forward direction towards the so-called C-side. It features a non-superconducting dipole magnet (blue), tracking planes (pink and dark blue) and absorbers (dark gray). The Inner Tracking System (ITS, green) is the innermost detector and surrounds the interaction point. It is surrounded by the Time Projection Chamber (TPC, blue), the Transition Radiation Detector (TRD, yellow) and Time Of Flight (TOF, orange). These detectors cover and azimuthal angle of 360°. The pseudorapidity acceptance is at least $|\eta| \leq 0.84$ at any azimuthal angle. Even further outside, there are several calorimeters installed (light blue). These do however cover only a fraction of the azimuthal angle. [Aam+08]

4.3 The ALICE Inner Tracking System

The detector system closest to the interaction point in ALICE is the Inner Tracking System (ITS). It is a silicon-based detector optimized for tracking, especially precise determination of the track impact parameter. This parameter quantifies the ability to separate the primary vertex and secondary vertices of a collision. A good track impact parameter resolution is beneficial for the study of heavy-flavor decays, as their lifetime and thus their time-of-flight in the detector is very short. [Mus19] The mean lifetime of a Λ_c is about $(202 \pm 3) \cdot 10^{-15}$ s [Wor+22]. At approximately the speed of light, this gives a mean decay length of about (60.5 ± 0.8) µm. For the Λ_c, in order to differentiate primary and secondary vertex, the track impact parameter resolution needs to be lower than this. Increasing the track impact parameter resolution will enhance heavy-flavor production measurements, but also other observables as low-mass dielectrons [Col22b].

4.3.1 ITS

The first iteration of the ALICE Inner Tracking System (ITS, for clarity referred to as ITS1) was made up by silicon semiconductor detectors arranged in different shapes and six individual layers. The innermost two layers were Silicon Pixel Detectors (SPD), followed by two Silicon Drift Detectors (SDD). The ITS1 was finished by two layers of Silicon Strip Detectors (SSD). A schematic drawing of the detector layers is given in figure 4.3. While the SPD provided only

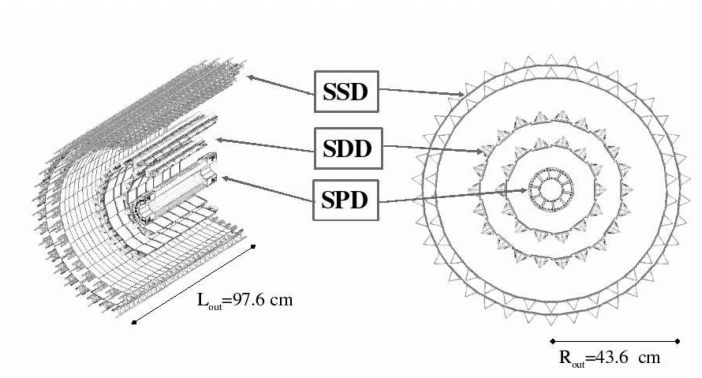


Figure 4.3: Sketch of the original ALICE ITS as it was present during LHC run 1 and 2. Taken from [Aam+08].

a binary signal for trajectory determination, the SDD and SSD could additionally be used for particle identification (PID) via energy loss $\mathrm{d}E/\mathrm{d}x$ in low-p_T ranges [Abe+14]. Table 4.1 shows the dimensions of the several layers present in ITS1. To be noted is also the radiation length of 1.1 % X_0. This was, at the time of construction, already the lowest for all LHC experiments [Abe+14].

Table 4.1: Dimensions for the ITS1 subdetectors. Taken from [Aam+08].

Layer	Type	r (cm)	$\pm z$ (cm)	Area (m^2)	Channels
1	pixel	3.9	14.1	0.07	3 276 800
2	pixel	7.6	14.1	0.14	6 553 600
3	drift	15.0	22.2	0.42	43 008
4	drift	29.7	29.7	0.89	90 112
5	strip	43.1	43.1	2.20	1 148 928
6	strip	48.9	48.9	2.80	1 459 200
Total				6.52	12 571 648

4.3.2 ITS2

The ITS1 remained in operation for LHC Run 1 (2009-2013) and Run 2 (2015-2018), until it has been decommissioned and replaced by the ITS2 during LHC Long Shutdown 2 (LS2, 2018-2022). The ITS2 features new silicon detector layers consisting of Monolithic Active Pixel Sensors (MAPS) named ALPIDE. The detector compromises 7 layers of quasi-quadratic pixel of approximately 29 µm × 27 µm. The dimensions of every layer are noted in table 4.2. A schematic overview about the detector layers is given in figure 4.4. The three innermost layer form the Inner Barrel (IB) while the outermost 4 layer are called Outer Barrel (OB). The ALPIDE chips have a thickness of 50 µm in the IB and 100 µm in the OB, while the ITS1 used silicon chips with a thickness of 350 µm. This leads to heavily reduced radiation length, especially in the IB, where $\approx 0.35\,\%\ X_0$ per layer are achieved. The OB modules

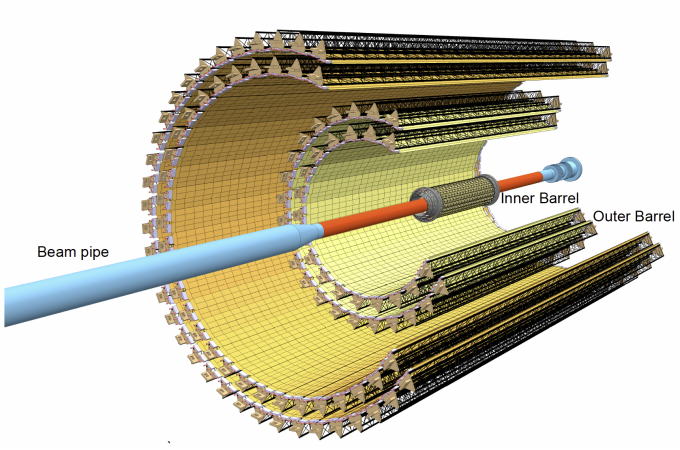


Figure 4.4: Schematic view of the ALICE ITS2 as it was installed during LHC LS2 and in use during LHC run 3. Taken from [Abe+14].

lower the radiation thickness to $\approx 1\,\%\ X_0$ per layer. In total, the radiation length of the ITS2 is lowered by roughly one quarter with respect to the ITS1 while even containing an additional layer. The distance between the interaction point and the innermost layer could be reduced from 3.9 cm to 2.2 cm. While the active area has been increased by about 30% from 6.52 m^2 to 9.28 m^2, the number of channels has increased been increased by three orders of magnitude from approx. 12.6 million to approx. 12.6 billion. Therefore, the average pixel density is heavily improved. [Abe+14]

The spatial resolution of the ITS1 was in the order of tens of µm, being lower in the layer close to the interaction point. The ITS2 features 5 µm in all layers and directions. Reduced radiation length, reduced distance to the interaction point and increased spatial resolution are expected to increase the track position resolution of the primary vertex by a factor of three or even higher. As mentioned in section 4.3.1, the ITS1, specifically SDD and SSD, were capable of PID via specific energy loss. During ITS upgrade studies, it was found that the availability of PID capabilities comparable to ITS1 have only little effect on several analyzed benchmark channels. It was therefore decided to not include a dedicated energy measurement in the readout. Approaches to still realize an energy resolution by special readout techniques are currently under investigation. The redesign of the complete readout chain enables the ITS2 to operate with a maximum rate of 100 kHz in Pb-Pb collisions and 400 kHz in pp collisions. This is an improvement by two orders of magnitude compared to the ITS1 with maximum rate of 1 kHz and about a factor of two higher than needed for the ALICE upgrade [Abe+14].

Technically, the chips are mounted on staves of carbon foam providing a support structure. Behind the chips, a cold plate from carbon fiber is mounted. Through this cold plate, cooling water is circulating to dissipate the heat away from the detector. Electrical interconnection

Table 4.2: Dimensions for the ITS2 subdetectors. Layer 0, 1, 2 make up the Inner Barrel (IB), Layer 3, 4, 5, 6 make up the Outer Barrel (OB). Taken from [Abe+14].

Layer	Type	r (cm)	$\pm z$ (cm)	Area (m^2)	Channels
0	pixel	2.24	11.78	0.04	56 623 104
1	pixel	3.01	11.78	0.06	75 497 472
2	pixel	3.78	11.78	0.07	94 371 840
3	pixel	19.44	21.08	1.05	1 409 286 144
4	pixel	24.39	21.08	1.31	1 761 607 680
5	pixel	34.23	36.88	3.21	4 315 938 816
6	pixel	39.18	36.88	3.67	4 932 501 504
Total				9.28	12 645 826 560

is achieved by mounting the chips onto a Flexible Printed Circuit (FPC) from polyimide. Additionally, a little amount of passive components like decoupling capacitors is mounted to the FPC. [Abe+14]

4.3.3 ITS3

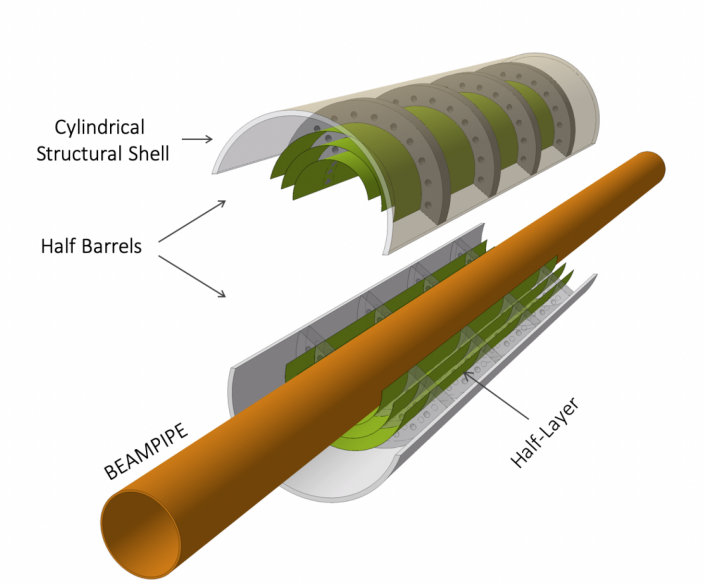


Figure 4.5: Schematic view of the ITS3 Inner Barrel foreseen to be installed in LHC LS3. Each of the six half layers (green) will be made up of a rectangular part of a single wafer. Taken from [Mus19].

During the LHC Long Shutdown 3 (LS3) in 2026-2028 the ALICE ITS2 will be upgraded to the ITS3. In particular, the ITS2 Inner Barrel will be replaced by an entirely redesigned detector. The Outer Barrel will however stay in place. Therefore, ITS3 refers mainly to the to-be-upgraded IB here. While the ITS2 IB consists of rectangular sensors mounted on staves, the ITS3 will be constructed of only six waver-scale chips with close to no additional

material apart from silicon. This will lead to a great reduction of material budget in the most sensitive region of the whole ALICE experiment. [Mus19] A schematic drawing of the planned inner barrel design is given in figure 4.5.

Table 4.3: Proposed dimensions for the ITS3 layers listed in the Letter of Intent (LoI). Note that these values are still to be confirmed for the final detector design. The number of channels is a rough estimation based on the proposed pixel size of 15 µm × 15 µm. Layer 3-6 are identical with the ITS2 from table 4.2. Taken from [Mus19].

Layer	Type	r (cm)	$\pm z$ (cm)	Area (m^2)	Channels
0	pixel	1.8	13.50	0.03	135 000 000
1	pixel	2.4	13.50	0.04	181 000 000
2	pixel	3.0	13.50	0.05	226 000 000

The proposed dimensions for the ITS3 are listed in table 4.3. It should be noted that these values originate from the Letter of Intent for the ITS3, which has been published fairly early in development. Exact values may still change towards the final detector.

The three key points to lower the material budget further with respect to the ITS2 are:

- Removing the need for water cooling by lowering the power consumption
- Removing the carbon space frame by bending the wafer to an intrinsically stiff half layer shape
- Removing the need for a FPC (within the acceptance region) by using stitched sensors on a single wafer per half layer

In the following, these three key ingredients and their challenges will be discussed briefly. In an R&D effort for the ITS2, it was found that air cooling becomes a realizable option if the power consumption of the sensor lies below 20 mW cm^{-2} [Mus19]. It still has to be studied, whether this is achievable within the *TPSCo.* 65 nm CMOS technology. Due to process limitations, a whole wafer-scale chip can not be produced at once. Instead, the wafer is filled with repetitive sensors units which are designed such that they can be daisy-chained by adjacent placement. This technology is well established for CMOS processes as they are used here [Mus19]. However, stitching of CMOS MAPS has never been demonstrated in high-energy physics so far[1]. Multiple stitching allows to produce large detector parts on a single wafer, without having the need to create mechanical and electrical interconnections separately. For the ITS3, it is envisaged to form detector layers from two half layers each. By geometrical considerations, length of the barrel, diameter of the final detector and diameter of the wafer are in a trade-off. With the 200 mm wafers of the *TowerJazz* 180 nm process, options are rather limited, as either the diameter or the length would severely suffer. It

[1] July 2023

is therefore planned to switch to the *TPSCo.* 65 nm CMOS process, which uses 300 mm wafers. Thus another R&D challenge for the ITS3 is to qualify this new technology for usage in high-energy physics in terms of efficiency, spatial resolution, radiation hardness and so forth. The last missing ingredient is bending of the silicon wafers in order to have an intrinsically stiff shape making it possible to get along without additional support structures within the detector acceptance window. Bending has already successfully been demonstrated with ALPIDE chips of the ITS2 [Pro22]. For the new 65 nm technology, the verification is currently ongoing. [Mus19]

To sum up, the transition from the *TowerJazz* 180 nm process to the *TPSCo.* 65 nm process is a crucial step in view of the ITS3 project. This work is meant to contribute to this validation efforts of the 65 nm technology in high-energy physics, mainly focused around studies of radiation hardness of certain sensor prototypes.

5 The MLR1 Test System

The ALPIDE chip for the ALICE ITS2 was fabricated in the *TowerJazz* 180 nm process. For the ITS3, the usage of the *TPSCo.* 65 nm process is intended. One important reason for this particular technology is the wafer size of 300 mm in diameter in contrast to the 200 mm wafers used for the 180 nm process. Only this step enables the fabrication of wafer-sized particle trackers suitably large for usage in the ALICE ITS. [Sno+23] The MLR1 (Multi-Layer Reticle 1) is the first submission of test structures fabricated for the ITS3 project. It features several pixel detector test structures as well as others such as transistor test structures. The MLR1 was designed within the CERN EP R&D group on monolithic pixel sensors and thus also contains test structures for projects other than ITS3. [Sno+23] One main goal of this first submission was measuring the maximum reachable detection efficiency of fresh chips as well as after irradiation to radiation doses beyond the expectation for the projected lifetime of ITS3. In the same context, the radiation hardness of the *TPSCo.* 65 nm CMOS technology is also probed to qualify it as a potential technology node for the ALICE 3 project [Col22a].

To this point, different chips are available from four different wafers. The different wafers were gradually modified on doping levels of various implants. In this work, solely chips from Wafer 22 are used. This wafers offers the highest level of process optimization. [Sno+23]

The MLR1 submission contains a variety different of versions of Analogue Pixel Test Structures (APTS) featuring different pixel pitches (10 µm, 15 µm, 20 µm and 25 µm), different in-pixel electronics and different amplifier circuitry to study the analog response of the pixel design. The pixel matrix offers only 4×4 pixels of which the analog output can be read out individually for every pixel. Moreover, the large phase space of different features allows detailed studies on charge collection. [Mag22]

5.1 Digital Pixel Test Structure (DPTS)

The Digital Pixel Test Structure (DPTS) fixes a single pixel pitch of 15 µm as well as one single front-end circuit design. The advantage of this prototype lies in the size of the pixel matrix featuring 32×32 pixel and thus an active area of $480\,\mu\text{m} \times 480\,\mu\text{m}$. It is therefore comparably easy to get significant results on the overall detector performance. In contrast

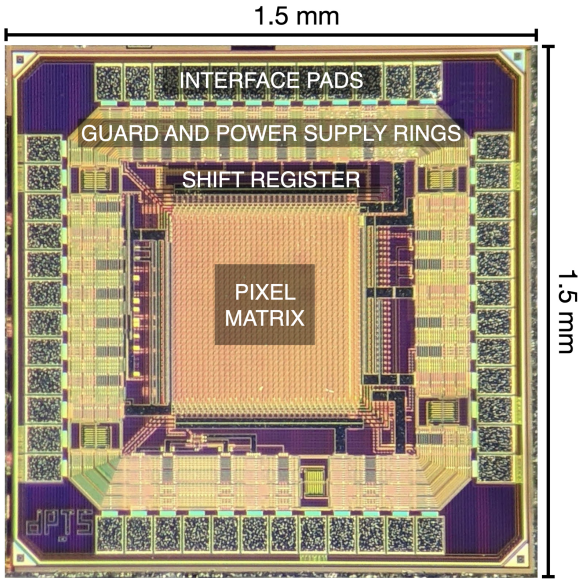


Figure 5.1: Microscope image of the DPTS chip. Taken from [Agl+23, Fig. 1(b)].

to the APTS, the DPTS provides only a single readout line giving binary information for all pixel combined. The position of hits is time-encoded. Technically, the output line is realized following the CML standard thus having two electrical connections, of which one transmits the original signal and the other a logically inverted signal of the original signal. [DPT21]

Additionally, the Time-over-Threshold (ToT) can be obtained from the output line. This can be used to quantify the charge deposited in the sensor because both quantities are proportional in first order (for more details, see section 6.5). Figure 5.1 shows a microscope image of the DPTS. The pixel matrix is visible in the center of the chip. A shift register is placed in the vicinity of the pixel matrix. Guard and power supply rings surround both the matrix and the shift register. On the edge of the pixel, interface pads can be seen. The chip is glued to a carrier PCB and the electrical connection is achieved through wire bonds between the interface pads on the chip and the corresponding pads on the carrier PCB. [DPT21] There is a total of only three different versions called X-, S- and O-Type. The front-end of the pixel remains unchanged through all versions, but there are differences in the readout, which will be explained in the following [DPT21].

Pixel Design

Figure 5.2 shows the cross section of a pixel as used in the DPTS. The P^+-doped substrate is the initial silicon wafer. Before processing, the wafer has a thickness in the order of 500 µm [Spi05]. On top of the substrate, a less doped high-resistivity layer is grown forming an epitaxial silicon layer. The thickness of this layer is estimated to be $O(10\,\mu m)$ [Sno+23]. A

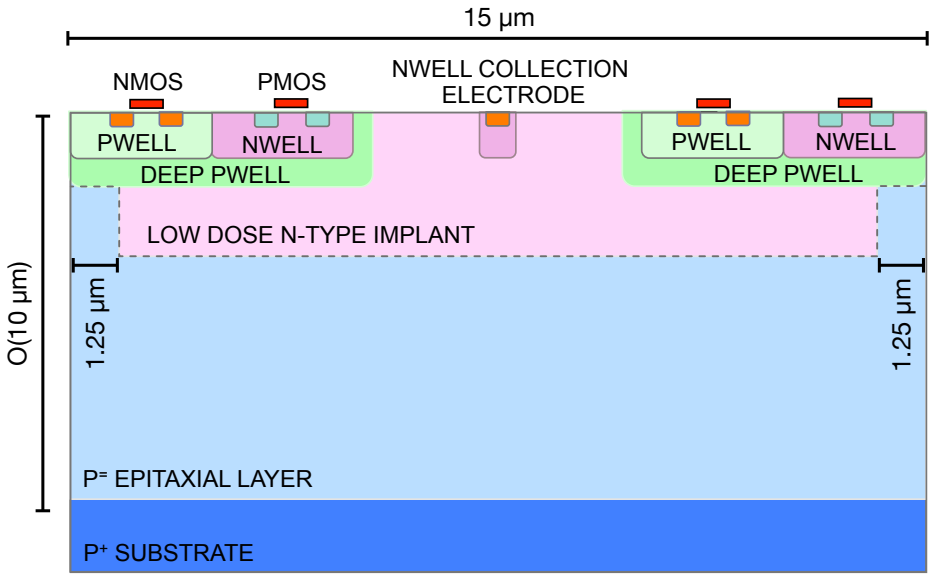


Figure 5.2: Cross section of a single pixel of the DPTS. Not to scale. Taken from [Agl+23, Fig. 1(a)].

collection electrode is placed in an n-doped well in the center of the pixel. The $P^{=}$-epitaxial layer and the n-doped well form a depletion region around the collection electrode. To extend the depletion region, a low dose n-type implant is implemented in the upper part of the sensor, reaching almost up to the pixel borders. This enlarges the depletion region in a plane parallel to the wafer. The low dose n-type implant extends only up to 1.25 µm towards the pixel border, which creates an electric field perpendicular to the wafer plane. Both modifications cause faster charge collection as the amount of charge carriers moved by drift is increased. Furthermore, this reduces charge sharing, which leads to a higher sensitivity at the cost of reduced spatial resolution. [Agl+23; Spi05]

Towards the border of the pixel, the front-end transistors are hosted in shielding deep p-doped wells. An insulating silicon dioxide (SiO_2) layer and metal traces on top of the wafer enable construction of PMOS and NMOS transistors. Therefore, standard CMOS circuits can be realized in the same device. Within the deep p-doped well, NMOS transistors are embedded in a p-doped well and PMOS transistors are embedded in an n-doped well. [Agl+23]

As the overall charge collection is dominated by drift within the depletion region in the epitaxial layer, the majority of the substrate serves no other purpose than providing mechanical support. Process standardization, makes it impossible to have thinner wafers in the first place. However, it is possible to thin down the final sensor to a total thickness of approximately 50 µm by grinding down the substrate layer. [Mag22]

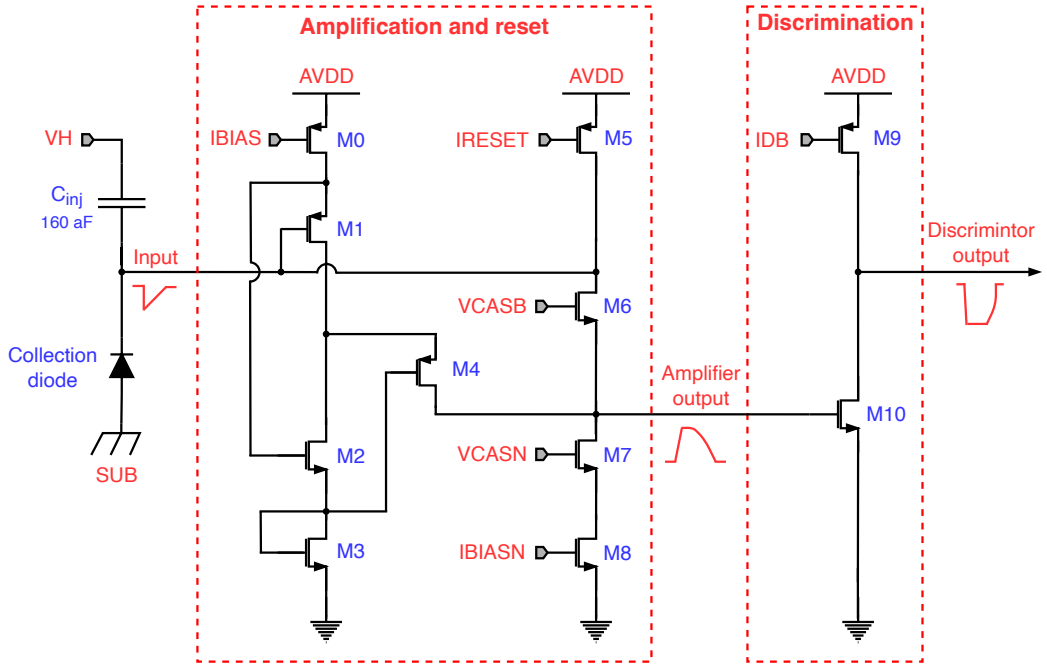


Figure 5.3: Schematics of the DPTS in-pixel circuit. Taken from [Agl+23, Fig. 3].

Front-End

In figure 5.3, the front-end of the DPTS pixel is shown. This circuit diagram includes the amplification of the diode signal, the sensor reset and the discriminator. The address generation circuit is not shown here. A total of 10 transistors `M1-M10` is present in every pixel of the matrix to realize the three steps. The gate of transistor `M1` is the main input and directly coupled to the collection diode. It is connected as a source-follower (i.e. an amplifier, where the source is used as output) with a close to unity voltage gain. The output voltage is thus close to the input voltage. `M0` is controlled by I_{bias} and biases `M1` properly. The gate of `M2` is connected to the source of `M1`. It acts as common-source (i.e. an ampflifier, where the source is not used as input or output). This gives an inverting amplifier. Transistor `M3` is diode-connected and inserted between the source of `M2` and ground. This increases the operational margin of the amplifier. Transistor `M4` creates a second amplification stage effectively forming a cascode circuit. The secondary branch of the cascode is biased by I_{biasn}. [Pir+23]

An incoming particle will create free charge carrier in the diode. By drift of these charge carriers a current is flowing. As the collection diode has a certain capacitance which will be charged and a voltage $\Delta V_{\text{signal}} = Q_s / C_{\text{sensor}}$ can be measured. The signal charge Q is usually in the order of $100\,e$. The sensor capacitance C_{sensor} should be low in order to have a large signal. [Pir+23]

V_{casb} in combination with `M6` creates a feedback mechanism for the amplifying stage in order to operate the amplifier at an optimal working point. Moreover, the feedback circuit injects

I_{reset} via `M5`, which is used to reset the diode after an incident particle. V_{casb} and I_{reset} control the baseline of the amplifier output via their transistors and the feedback circuit. `M9` and `M10` form a common-source stage, effectively giving a current comparator. The pixel output is pulled to high level by `M9` until the input current of `M10` is larger than the input current of `M9`, which is I_{db}. Overall, the threshold of the sensor is thus controlled by tuning I_{reset}, V_{casb} and I_{db}. [Pir+23]

Additionally to the 1024 pixel, the DPTS has a separate analogue monitor pixel next to the matrix. The front-end of this pixel is the same as for the digital pixel, with the exception that the discriminator stage is replaced by an amplifier. This enables studies of the analogue waveforms in order to optimize biasing parameters. [DPT21]

Readout and Slow Control

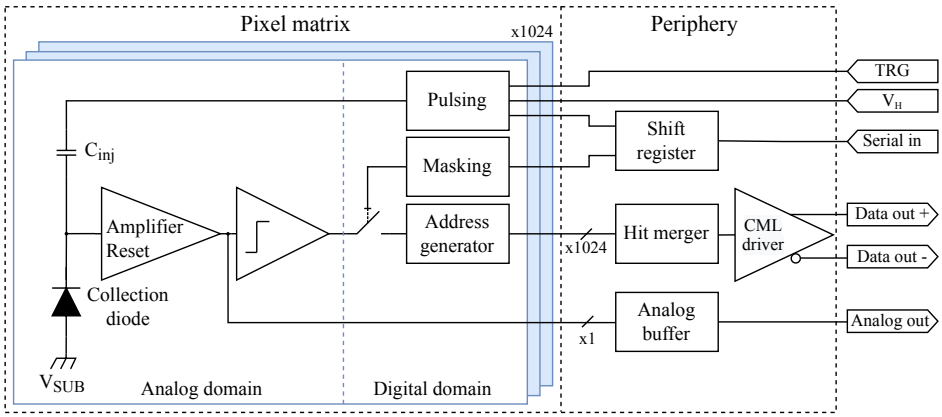


Figure 5.4: Functional diagram of the the DPTS. Not shown here is the biasing, which is directly applied to the amplifier-reset and discriminator block in the analog domain. Taken from [Agl+23, Fig. 2].

A functional diagram of the DPTS readout and slow control is given in figure 5.4. The amplifier-reset and discriminator blocks were described in the previous section. Furthermore, every pixel features a block for pulsing, which is controlled by a global pulsing voltage V_{h}, a global trigger signal TRG and pixel-specific activation bits controlled by the peripheral shift register. Thus, every pixel can individually be pulsed with a certain voltage V_{h} triggered by a signal in the TRG input. The pulsing itself is performed through an injection capacitor with a nominal value of 160 aF. [DPT21]

Furthermore, there is a masking section in the shift register. Masking makes it possible to deactivate noisy pixel by switching off their discriminators. 3×32 bit are used for this in the shift register. The sections `MC[31:0]`, `MR[31:0]`, `MD[0:31]` mask columns, rows and diagonals respectively, when their value is set to 1. An individual pixel is only masked (deactivated),

when its column, row *and* diagonal are set to be masked. Therefore, it is not possible to *unmask* a single pixel on its own. Furthermore, when trying to mask more than one pixel, ghost-masked pixel can appear, if the combination of columns, rows and diagonals is set in a certain way. The probability for having ghosts increases with the number of pixels masked. For reasons of redundancy, every bit is present 3 times in the shift register. Overall, this leads to a total of $3 \cdot (2 \cdot 32 + 3 \cdot 32) = 480$ bit in the shift register. [DPT21]

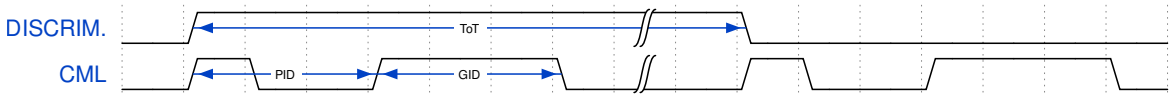


Figure 5.5: Logic diagram of the input and output pulses of an address generator in a DPTS pixel. Taken from [Agl+23, Fig. 4].

The discriminated signal is being processed by an address generator. This generator produces pulses with time-encoded pixel column and row information for each rising *and* falling edge of the discriminator stage. The output pulse shape looks as shown in figure 5.5. In particular, the duration T_{PID} of the PID pulse encodes the PID, which is correlated to the row of a pixel. The duration T_{GID} of the GID pulse encodes the GID, which is correlated to the column. In particular

$$T_{PID} = T_H + \delta_P \cdot PID \tag{5.1}$$

$$T_{GID} = T_0 + \delta_G \cdot GID, \tag{5.2}$$

where $T_H \approx 4.4\,\text{ns}$ and $T_0 \approx 1\,\text{ns}$ are fixed offsets and $\delta_P \approx \delta_G \approx 150\,\text{ps}$ are the time steps of the encoding. [DPT21] These values are nominal and may change with changing operating conditions, such as biasing parameters, temperature, back bias V_{bb} or chip-to-chip.

Row ↓\ Col→	0	1	2	3	4	5	6
0	0 0	1 0	2 31	3 31	4 0	5 0	6 3
1	0 1	1 1	2 30	3 30	4 1	5 1	6 3
2	0 2	1 2	2 29	3 29	4 2	5 2	6 2
3	0 3	1 3	2 28	3 28	4 3	5 3	6 2
4	0 4	1 4	2 27	3 27	4 4	5 4	6 2
5	0 5	1 5	2 26	3 26	4 5	5 5	6 2
6	0 6	1 6	2 25	3 25	4 6	5 6	6 2
7	0 7	1 7	2 24	3 24	4 7	5 7	6 2
8	0 8	1 8	2 23	3 23	4 8	5 8	6 2
9	0 9	1 9	2 22	3 22	4 9	5 9	6 2
10	0 10	1 10	2 21	3 21	4 10	5 10	6 2
11	0 11	1 11	2 20	3 20	4 11	5 11	6 2

(a) O-Type (PID Flip)

Row ↓\ Col→	0	1	2	3	4	5	6
0	0 0	1 0	2 31	3 31	4 0	5 0	6 31
1	1 1	0 1	3 30	2 30	5 1	4 1	7 30
2	0 2	1 2	2 29	3 29	4 2	5 2	6 29
3	1 3	0 3	3 28	2 28	5 3	4 3	7 28
4	0 4	1 4	2 27	3 27	4 4	5 4	6 27
5	1 5	0 5	3 26	2 26	5 5	4 5	7 26
6	0 6	1 6	2 25	3 25	4 6	5 6	6 25
7	1 7	0 7	3 24	2 24	5 7	4 7	7 24
8	0 8	1 8	2 23	3 23	4 8	5 8	6 23
9	1 9	0 9	3 22	2 22	5 9	4 9	7 22
10	0 10	1 10	2 21	3 21	4 10	5 10	6 21
11	1 11	0 11	3 20	2 20	5 11	4 11	7 20

(b) X- and S-Type (PID Flip and Cross Connect)

Figure 5.6: Upper left corner of the pixel matrices of both chip layouts. The first number in each cell represents the pixels GID and the second number the PID.

The assignment of (GID, PID) pairs to physical (column, row) pairs is determined by the chip version. In simple terms, for the initial assignment, PID is approximately equal to the row number, and GID is approximately equal to the column number. The pixel (c=0, r=0) is located in the upper left corner of the matrix and has $PID = 0$. The same applies to the pixel immediately to the right. Moving to the right from there, the next two pixels have $PID = 31$, which reverses the numbering of PIDs from bottom to top within the column, rather than top to bottom. This pattern continues across the chip.

Additionally, every second column introduces a slight delay of approximately a few nanoseconds. This delay reduces the likelihood of neighboring pixels emitting their pulses simultaneously, which could lead to interference or collisions. This collision avoidance strategy is particularly important when multiple pixels within a cluster fire their pulses at the same time.

In O-type chips, the GID corresponds directly to the column number, as depicted in figure 5.6a. For X- and S-type chips, a cross-connection scheme is employed. In these chips, every second row swaps the outputs of neighboring pixels. Consequently, when examining all pixels with $GID = 0$ in ascending PID order, one will find that the first pixel is in the first physical column, the second pixel is in the second column, the third pixel is in the first column, and so forth. This configuration is visually represented in figure 5.6b.

To achieve this, the data line between the discriminator and address generator is exchanged for these adjacent pixels. Nonetheless, pulsing and masking operations continue to be executed based on the physical (col, row) coordinates of the pixel. This implementation of the cross-connection scheme aims to mitigate readout line collisions between vertically adjacent pixels. With this scheme in place, there is always a short readout delay separating two neighboring pixels.

The S-type variant is equivalent to the X-type, with the exception of having the ground connections of the analog and digital power domains shorted. [DPT21] Operational differences between all three sensor versions turned out to be negligible [Sno+23]. Thus, their results are treated equivalently in this work. Lastly, the analog pixel bypasses the discriminator by leading its signal directly into an analog buffer and towards the analog output of the chip.

An oscilloscope capture of real output pulses is shown in figure 5.7. There, the analog waveform of the monitor pixel is shown in blue and the corresponding CML output is shown in yellow (non-inverted) and purple (inverted). It has to be noted that the ToT is usually three orders of magnitude longer than the assertion or deassertion pulse itself. Therefore, a waveform with decreased time base is shown on the right of figure 5.7. The 4 characteristic edges of the pulse can be seen.

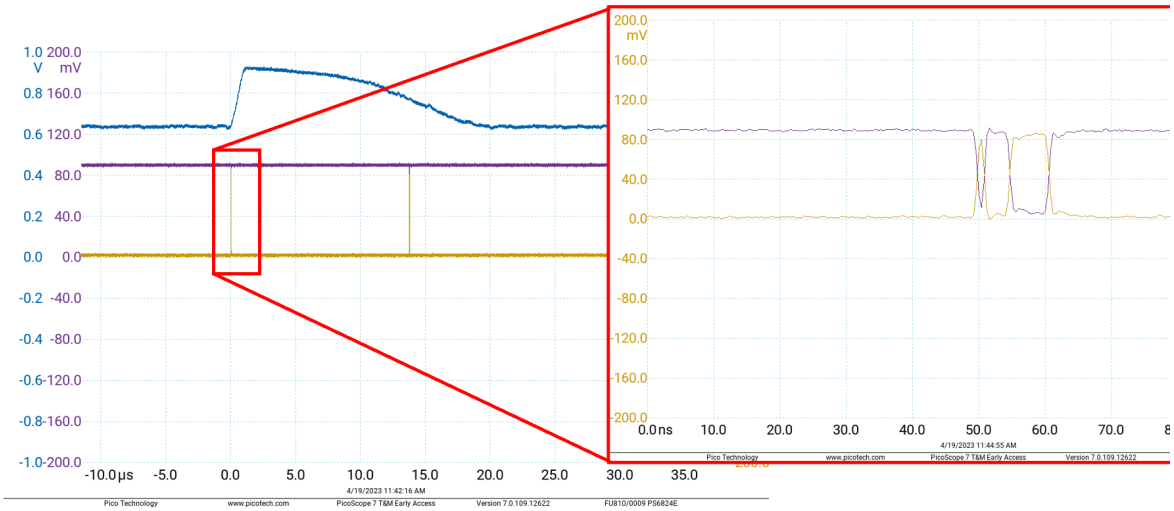


Figure 5.7: Exemplary waveform of the non-inverted (yellow) and inverted (purple) CML output as well as the analog waveform of the monitor pixel (blue). The time base in the left plot is 5 µs /div. and 10 ns /div. in the right plot. The right plot is therefore zoomed in time-direction by a factor of 500.

5.2 Test System

The chip bias voltages and currents depicted in figure 5.3 are provided by the data acquisition system (DAQ). Specifically, the DAQ system for all MLR1 structures consists of a designated DAQ board with USB 3.0 connection. As the DAQ board was originally designed for testing the ALPIDE chips, testing of MLR1 chips requires an adapter called proximity board. The proximity board hosts digital-analog converters (DAC) for providing voltage and current biases to the chip as well as level shifters to convert from 3.3 V logic level of the DAQ board FPGA to the 1.2 V logic level of the chip. For certain chip types (for example APTS), analog-digital converters (ADC) are placed on the proximity board too. In case of the DPTS, such ADCs are not needed. There exists also a DPTS breakout board (BoB), which features potentiometers instead of DACs and test points for all data and biasing lines for manual operation. The readout lines of the chip are fed directly to an oscilloscope to cope with the very short ($\mathcal{O}$(ns)) pulses. Thus, the DAQ board is used only to control the DACs for biasing and to control the shift register on the chip for masking and pulsing.

The analog output of the monitoring pixel can be accessed via a connector on the proximity board. Reverse bias to SUB and PWELL can be delivered via connectors on the DAQ board. Additionally, the DAQ board offers a trigger output which gives a pulse when pixel on the matrix are pulsed via charge injection. This can be used to trigger oscilloscope captures. The trigger output is not asserted when pixel on the matrix fire due to real particles or fake-hits. In case of beam tests or source scans, a trigger on the CML output signal or an external

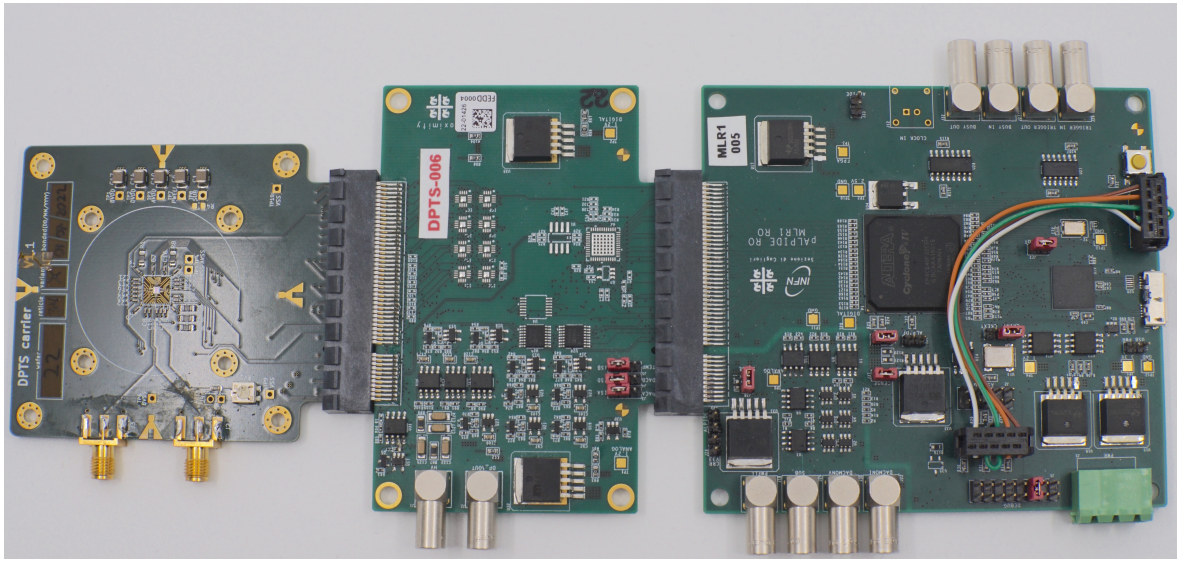


Figure 5.8: Image of chip carrier, proximity board and DAQ board. The chip can be seen as small shiny square in the middle of the carrier card.

trigger, such as a scintillator, has to be used. Lastly, the other in- and outputs of proximity and DAQ board are not used for DPTS operation.

To achieve mechanical and electrical connection, the chip itself is glued and wire-bonded to a carrier card. The carrier card mainly serves the purpose of handleable objects. Apart from that, only a small number of decoupling capacitors, a variable resistor and two SMA connectors for the output lines are mounted.

Figure 5.8 gives an overview of the three main components of the MLR1 DAQ system. The carrier card on the very left holds the chip to test. The proximity board can be seen in the middle and the DAQ board is the rightmost part. The interconnection between carrier card, proximity board and DAQ board is achieved trough custom-layout PCIe x8 connectors.

6 Experimental Setup

For laboratory measurements with the DPTS, there is a standard setup used in most cases. This setup is always used unless noted differently. Figure 6.1 shows the default connections of the carrier board and DAQ board towards other systems. The DAQ board is powered with 5 V provided by a *Rohde&Schwarz HMP4040* laboratory power supply. For control of the chip, the DAQ board is connected to a PC via a USB 3.0 cable. Back bias to the PWELL and SUB pads of the chip is provided from another channel of the same power supply trough a capacitive filter board, the DAQ and proximity board to the chip. Additionally, the power supply is connected via USB to the PC to automatize scanning over different PWELL and SUB voltages. Both readout lines of the chip are connected to two input channels of a *Pico Technologies 6000 Series*, where the coupling is set to DC 50 Ω. Either a *6406E* or a *6804E* is used, which have a maximum bandwidth of at least 500 MHz. When pulsing pixels, the DAQ board provides a trigger signal, which is fed into the auxiliary trigger input of the oscilloscope.

The back side of the carrier card is covered partially with an aluminium cooling jig through which temperature-controlled water circulates. The cooling water is provided by a *HUBER Minichiller 280 OLÉ* or a *HUBER Minichiller-H1 plus* which can both cool water down to −20 °C. The latter is also able to heat the water up to 40 °C. To avoid any condensation on the chip, the temperature is kept at 5 °C minimum above the dew point in the laboratory. Ambient temperature and humidity are monitored by a *DRACAL PTH200* probe. Practically, this enables measurements down to 15 °C without having to keep the setup in a dry-box. Additionally, the cooling jig is equipped with a temperature probe in order to monitor the jig temperature more precisely. During the measurement, it is crucial to cover the chip light tight in order not to influence the charge collection in the chip by ambient light. The chips are optimized for measuring ionizing radiation, but it is, to a certain extent, also sensitive to visible light, because of the photo-effect.

In table 6.1 the nominal operating voltage and current biases are listed. The currents are provided via a current mirror with a fixed current ratio. This leads to differences in what is set by the DAC compared to what is actually flowing trough the front-end. The software framework is designed so that the front-end value of the current is always taken as input.

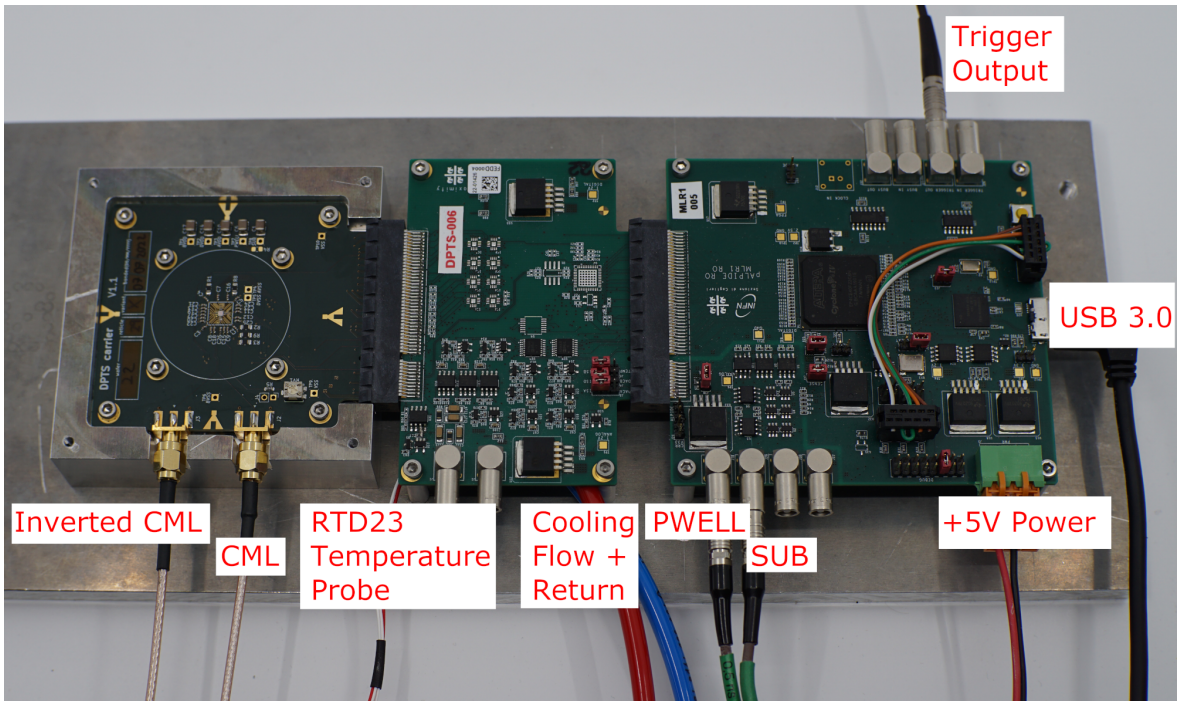


Figure 6.1: Standard setup for DPTS laboratory measurements.

Conversion to DAC currents is performed internally. For simplicity, listings of bias currents in this work always use the front-end values. The values are always applied to the chip, if not noted otherwise. An exception is I_{biasf}, which is only needed for operating the analog monitor pixel and set to 0 mA during regular digital operation of the sensor. To this date[1], the whole parameter space has not yet been explored. To reduce the parameter space, the ratio of $I_{\text{bias}}/I_{\text{biasn}} = 10$ is kept strictly in all measurements. Furthermore, the back biases V_{pwell} and V_{sub} are always shorted so that they can be referred to as general back bias voltage $V_{\text{bb}} := V_{\text{sub}} = V_{\text{pwell}}$.

A variety of different lab measurement techniques is used for all following studies. All scripts for data acquisition and basic analyses are collected in the repository `apts-dpts-ce65-daq-software`[2] within the CERN GitLab. The repository access is currently protected. Several people from the ITS3 project have contributed to the codebase.

6.1 Data Compression

The data coming from the CML outputs of the chip looks as described in section 5.1 and shown in figure 5.5 and figure 5.7. However, the only relevant information are the timestamps of the rising and falling edge of the non-inverted (equals to falling and rising edge of the

[1] July 2023
[2] `https://gitlab.cern.ch/alice-its3-wp3/apts-dpts-ce65-daq-software`

Table 6.1: Nominal values of current and voltage biases in the DPTS. Note that I_{biasf} is only needed for the analog pixel and set to 0 µA during regular digital readout. [Agl+23]

Description	Set by DAC	Current mirror ratio	Front-end
I_{reset}	10 µA	10^{-6}	10 pA
I_{bias}	10 µA	10^{-2}	100 nA
I_{biasn}	10 µA	10^{-3}	10 nA
I_{db}	10 µA	10^{-2}	100 nA
I_{biasf}	−4 mA	1	−4 mA
V_{casb}	300 mV		300 mV
V_{casn}	300 mV		300 mV
V_{h}	600 mV		600 mV
V_{pwell}	1.2 V		1.2 V
V_{sub}	1.2 V		1.2 V

inverted) signal. The size of data to be saved can be drastically decreased by performing online zero-suppression and saving only the timestamps of the edges. Since the edges have a finite rise and fall time, the timestamp of the edge is ambiguous and can be defined in different ways. When inverted and non-inverted signal are available (all lab measurements), the timestamp of an edge is linearly interpolated between the two data points at which the sign of (*non-inverted*) − (*inverted*) changes. Alternatively, if only the non-inverted signal is available, it is possible to fix a threshold and interpolate linearly between first point before and first point after rising above or falling below the threshold. Both methods work, while the first method is more accurate. Results from both methods are however not necessarily comparable.

6.2 Shift Register Test

A basic but important check of the chip operation is the shift register test. The shift register contains 480 bit which control pixel pulsing and masking (cf. section 5.1). The shift register test fills the shift register with repetitive patterns consisting of `00`, `11`, `10` and `01` subsequently with reading out the output afterwards. Such a test is considered passed if there is no mismatch between input and output within 1000 iterations over all four patterns. If the test does not pass, every further operation of this particular chip cannot be trusted, as it might be unknown what has really been written to the shift register. These chips are then strictly excluded from any further studies.

6.3 Monitor Pixel

In order to probe the large space of biasing parameters, it is often reasonable to take a look at the analogue output waveform. To do this, the `DP_AOUT` connector placed on the proximity board is connected to an oscilloscope channel with DC 50 Ω coupling. To activate this pixel, the masking bit `MD[0]` has to be asserted. This pixel will then respond to external stimuli or to the pulsing of pixel (c=31, r=31), even though the monitor pixel is besides the matrix.

6.4 Fake-Hit Rate Scan

Definition 6.4.1 (Hit)**.** *A pixel had a hit, if the discriminator output was logically high for a certain period and consequently assertion and deassertion pulse have been generated.*

Definition 6.4.2 (Fake-hit rate)**.** *The fake-hit rate is the rate of registered hits in a single pixel in absence of pulsing and external stimuli.*

To determine the fake-hit rate of a sensor, a series of N_{trg} trigger pulses is sent from the DAQ board towards the oscilloscope without actually pulsing any pixels on the matrix. Technically, this is achieved by sending the control to pulse the pixel matrix, without having any pixel selected via the shift register. The fake-hit rate, also referred to as noise occupancy, is then calculated as

$$FHR = \frac{N_{\text{hits}}}{n_{\text{pixel}} \cdot \Delta t_{\text{WF}} \cdot N_{\text{trg}}}, \tag{6.1}$$

where N_{hits} is the count of waveforms that show pixel hits, $n_{\text{pixel}} = 1024$ the count of all pixel on the DPTS matrix, Δt_{WF} the length of the recorded waveforms and N_{trg} the number of sent trigger signals by the DAQ board, thus the count of recorded waveforms. N_{trg} is usually set to 10 000 or 100 000 in a trade-off between statistical uncertainty and measurement time. In the measurement, the length of the waveform is set to $\Delta t_{\text{WF}} = 40.002\,\mu\text{s}$, of which 2 ns are recorded before arrival of the trigger signal. Pre-trigger samples ensure that the full rising edge of the signal is sampled properly. Therefore, the fake-hit rate is given in terms of fake hits per pixel per second. Next, the number of properly decoded trains is divided by two as every pixel will generate two trains per (fake-)hit, one for the pixel assertion and one for the deassertion. Bad trains (trains with a number of edges not equal to four) will be counted twice, as per observation, this mostly occurs when two trains overlap each other and the minimum separation between two neighboring trains falls below the limit of 20 ns. Thus, every bad train will be counted double when adding up the number of fake-hits. Considering that 1 is the minimum measurable amount of fake hits, one can calculate the sensitivity limit of this measurement. This leads to $2.44 \cdot 10^{-3}\,\text{pixel}^{-1}\,\text{s}^{-1}$ or $0.24 \cdot 10^{-3}\,\text{pixel}^{-1}\,\text{s}^{-1}$ when using

$N_{\mathrm{trg}} = 10\,000$ or $N_{\mathrm{trg}} = 100\,000$ respectively. Furthermore, the measurement range is limited by a cut applied during data-taking. If there are more than 1000 level crossings within a single waveform, the data taking will be stopped. Such high number of crossings are most likely not decodable anymore because the probability of having overlapping trains is very high. Furthermore, only the first 32 level crossings are actually saved to reduce the amount of disk space. As 32 level crossings can make up a maximum of 8 trains, which correspond to 4 fake-hits (assertion + deassertion pulse), the maximum detectable fake-hit rate lies in the range of $97.7\,\mathrm{pixel}^{-1}\,\mathrm{s}^{-1}$ for any N_{trg}. In fact, slightly higher fake-hit rates can also be observed when there are bad trains present, as bad trains are counted double. Since the result is rounded up to the next integer, a missing "good" train does not lower the fake-hit rate but the additional presence of a bad train increases the amount of fake-hits instead.

To estimate the uncertainty of the fake-hit rate measurement, it has to be accounted for statistical and systematic uncertainty. The statistical uncertainty is calculated as

$$\sigma_{\mathrm{stat.}} = \frac{\sqrt{N_{\mathrm{hits}}}}{n_{\mathrm{pixel}} \cdot \Delta t_{\mathrm{WF}} \cdot N_{\mathrm{trg}}}, \tag{6.2}$$

as fake-hits are expected to occur in a Poisson-distributed manner. The systematic uncertainty is dominated by the fact that there is always a certain chance that either the assertion pulse or the deassertion pulse falls just out of the acquisition window and the fake-hit rate gets underestimated. Thus to account for this, the upper limit of hits is called $N_{\mathrm{hits}}^{\mathrm{max}}$ and is equal to the number of trains because in the worst case, every train has its corresponding assertion or deassertion pulse outside of the acquisition window. Moreover, the minimum number of hits $N_{\mathrm{hits}}^{\mathrm{min}}$ is the number of waveforms that show any activity. This accounts for the fact that there is decoding done on the edges. Potentially, this could fail. But it is for sure that there was at least one fake-hit, if there is at least a single level crossing in a waveform. The systematic uncertainties are then calculated as

$$\sigma^{-}_{\mathrm{syst.}} = \frac{N_{\mathrm{hits}}^{\mathrm{min}}}{n_{\mathrm{pixel}} \cdot \Delta t_{\mathrm{WF}} \cdot N_{\mathrm{trg}}} \tag{6.3}$$

as well as

$$\sigma^{+}_{\mathrm{syst.}} = \frac{N_{\mathrm{hits}}^{\mathrm{max}}}{n_{\mathrm{pixel}} \cdot \Delta t_{\mathrm{WF}} \cdot N_{\mathrm{trg}}}. \tag{6.4}$$

The overall uncertainty of the fake-hit rate is then summed up to

$$\sigma^{\pm} = \sqrt{(\sigma_{\mathrm{stat.}})^2 + \left(\sigma^{\pm}_{\mathrm{syst.}}\right)^2}, \tag{6.5}$$

with σ^- and σ^+ being the lower and upper limits of the uncertainty.

In view of the ITS3, the acceptable fake-hit rate can roughly be estimated by using the acceptable fake-hit rate for the ITS2 from its technical design report (TDR). The TDR lists a maximum of $10^{-5}\,\text{pixel}^{-1}\,\text{event}^{-1}$ [Abe+14]. Combined with the maximum readout rate of 100 kHz [Mus19], this translates to $1\,\text{pixel}^{-1}\,\text{s}^{-1}$ and should give a broad estimation for the usability of a DPTS-like front-end for the ITS3. Including a safety factor, the fake-hit rate will in the end likely have to be lower than this, but $1\,\text{pixel}^{-1}\,\text{s}^{-1}$ is still used as a first benchmark.

6.5 Threshold Scan

Definition 6.5.1 (Threshold)**.** *The threshold of a pixel is the amount of charge that needs to be collected by a pixel in order to generate a hit in that pixel.*

The goal of the threshold scan is to determine the threshold in units of charge for every pixel in the matrix. Therefore, every pixel is subsequently pulsed n_{inj} times with different voltages V_{h}. Typically, $n_{\text{inj}} = 25$ is used. The conversion from pulsing voltage to injected charge is determined by the pulsing capacitance $C_{\text{inj}} \approx 160\,\text{aF}$ [DPT21]. The following approximation is used:

$$Q_{\text{inj}} = C_{\text{inj}} \cdot V_{\text{h}} \tag{6.6}$$

$$\Rightarrow Q_{\text{inj}}[\text{C}] = C_{\text{inj}} V_{\text{h}}[\text{V}] \tag{6.7}$$

$$\Leftrightarrow Q_{\text{inj}}[e] = \frac{C_{\text{inj}} V_{\text{h}}[\text{V}]}{e} \tag{6.8}$$

$$\Rightarrow Q_{\text{inj}}[e] \approx \frac{160\,\text{aF}}{1.60 \cdot 10^{-19}} \cdot V_{\text{h}}[\text{V}] = 1000 \cdot V_{\text{h}}[\text{V}] = V_{\text{h}}[\text{mV}] \tag{6.9}$$

In first order, the injected charge in electrons equals the pulsing voltage in mV. Figure 6.2 shows characteristic curves, called S-curves, obtained during a threshold scan. As the injected charge gradually increases, a rising fraction of injections actually triggers a hit in the pixel. Every S-curve represents the behavior of one pixel. If the pixel would behave perfectly every time, the resulting S-curves would be step functions. Due to noise, the steps functions are smeared out. The threshold and the threshold noise are obtained as mean and standard deviation of the derivative of these S-curves. The threshold mean of the whole matrix is consequently defined as mean of all pixel thresholds.

Another important use case for threshold scans is the calibration of the Time over Threshold (ToT). An increasing pulsing voltage V_{h}, and consequently an increasing injected charge Q_{inj} will lead to increasing ToT. This dependency is shown in figure 6.3. Over a wide range of V_{h},

the correlation is linear. However, at low V_{h}, where the injected charge Q_{inj} is close to the pixel threshold, the behavior is non-linear. Therefore, the ToT-vs-V_{h} curves are fitted with the empiric function

$$ToT = aV_{\mathrm{h}} + b - \frac{c}{V_{\mathrm{h}} - d} \tag{6.10}$$

with a, b, c and d being fit parameters. It can be observed that the spread of ToT for a single V_{h} is rather large. However, this is not an effect on the pixel level but it is caused by large pixel-to-pixel differences. Therefore, the fit is applied to data from every pixel individually, heavily increasing the accuracy as seen in the plot. When taking data with a source or with a particle beam, the collected charge is a priori unknown but the ToT of the hits can be recorded. Using this calibration, it is then possible to determine the characteristic voltage for every hit by inverting the fit function equation (6.10) and plugging it into the ToT. This voltage is referred to as "calibrated ToT". It has to be noted that this is not a real voltage which could be measured at any point of the front-end circuit. It is rather a tool to express what the pulsing voltage V_{h} has to be during pulsing in order to generate a hit with the same charge in the pixel.

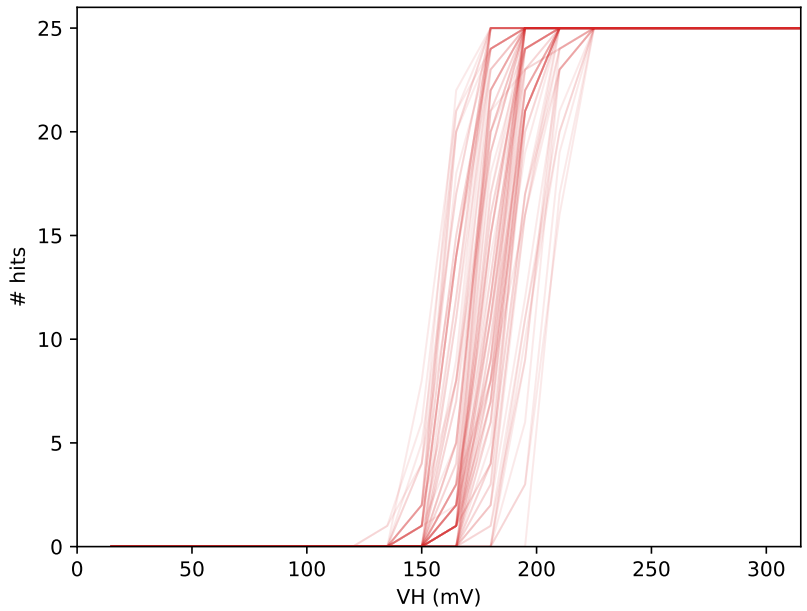


Figure 6.2: Example for S-curves from three rows of the DPTS matrix.

6.6 Decoding Calibration

Definition 6.6.1 (Decoding)**.** *Decoding describes the process of assigning measured (GID, PID) pairs to actual pixel coordinates in the (column, row) space.*

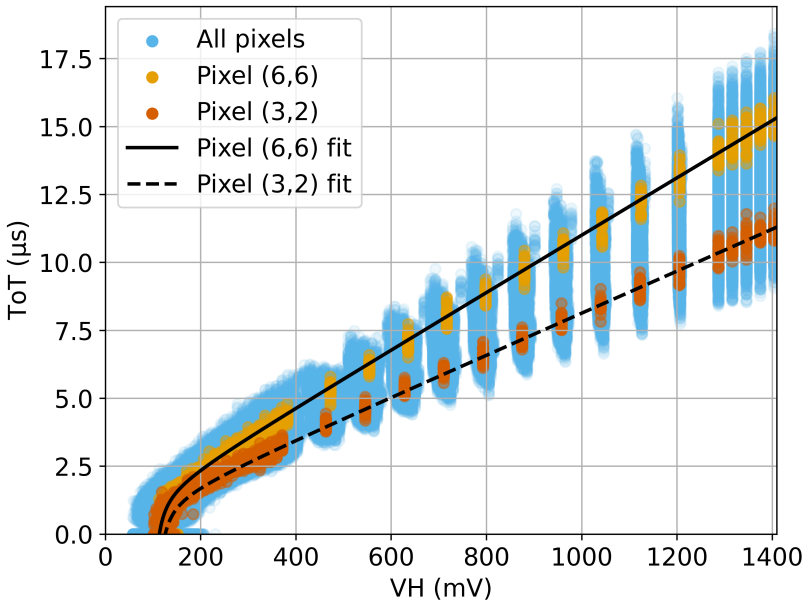


Figure 6.3: Example of a ToT-vs-V_h analysis. Orange and red data points represent results from a single pixel respectively. Solid and dashed show the fits applied to data from these pixels.

In order to use the hit information in form of (GID, PID) pairs, these have to be mapped to physical pixel coordinates in the sensor according to their position in the matrix. To obtain this mapping, a scan conceptually close to a threshold scan is performed. The only differences are that only a single value of $V_\mathrm{h} = 600\,\mathrm{mV}$ and more injections per pixel of $n_\mathrm{inj} = 100$ is used. One of those then gets a map of (GID, PID) pairs where 1024 clusters corresponding to the 1024 pixel are expected to form. The center of gravity (CoG) for every cluster is calculated, while rejecting 5% or at least one GID and one PID among the smallest and largest values. Since it is known which pixel is pulsed during pulsing, these CoGs can be associated to (column, row) pairs.

When taking data with real ionizing particles as in in-beam tests or during a source scan (cf. section 6.7), the position of the hit is obtained by finding the (GID, PID) cluster in the calibration map with the lowest distance between the cluster CoG and the (GID, PID) measured in the hit. The pixel coordinates (column, row) of this cluster are then assigned to the hit. Strictly speaking, there is one GID-PID map generated by (GID, PID) pairs obtained from the pixel assertion pulses (rising edge) and one map generated by pairs obtained by deassertion pulses (falling edge). Due to imperfection in the chip's address generation, these maps can differ quite substantially. Therefore, both CoG maps are saved and applied as the situation requires it. Measurements have shown that the calibrations rely quite heavily rely on the applied back bias V_bb, which makes it necessary to take decoding calibrations for every back bias that should be decoded. Influences from the other parameters, such as V_casb or

I_{reset}, have turned out to be negligible [Agl+23]. The operating point for taking decoding calibrations is therefore set to any set of biases, which allows a non-noisy operation. Finally, the decoding calibration was found to be temperature-dependent (see section 8.2). Therefore, best practice is to use a cooling jig whenever possible and to take decoding calibrations in-situ directly before or after collecting the data.

6.7 ^{55}Fe Source Scan

The script used for taking data with a ^{55}Fe is conceptually a derivative of the fake-hit measurement script. In contrast to this, the source scan sets the oscilloscope trigger on the rising edge of the non-inverted CML output of the chip. 70 mV is used as the trigger level. Apart from this, the length of the waveform is increased to $\Delta t_{\text{WF}} = 120.002\,\mu\text{s}$, while 2 ns are recorded before arrival of the trigger. The length is increased because higher charges in the pixel can cause higher ToT. During pulsing, the (injected) charge is limited to $\approx 1200\,e$ due to maximum V_{h}, while during a source scan, higher charges can be deposited and processed by the pixel. To analyze source data, the acquired and zero-suppressed waveforms are, together

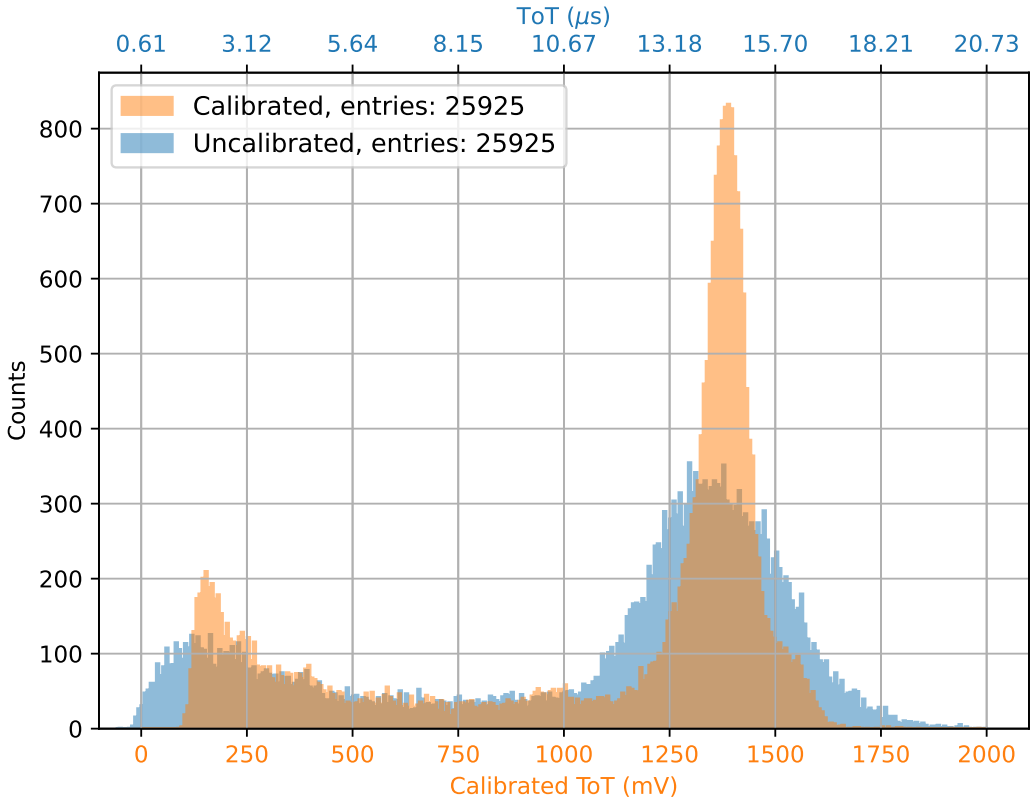


Figure 6.4: Example of an uncalibrated and calibrated ToT spectrum obtained from a ^{55}Fe scan.

with rising and falling edge decoding calibrations, fed into an analysis script. This script provides an algorithm to match assertion and deassertion of pixels within one waveform. The output from this script is a list of separate hits containing an event number, pixel column and row as well as the timestamp of the rising and falling edge for every hit. A following script processes this list and combines it with a ToT-vs-V_{h} calibration to obtain a corrected ^{55}Fe spectrum in terms of calibrated ToT (pulsing voltage equivalents, cf. section 6.5). Uncalibrated and calibrated spectra can be seen in figure 6.4. It is visible by how much applying the pixel-dependent ToT calibration improves the significance of the Mn-K$_\alpha$ peak.

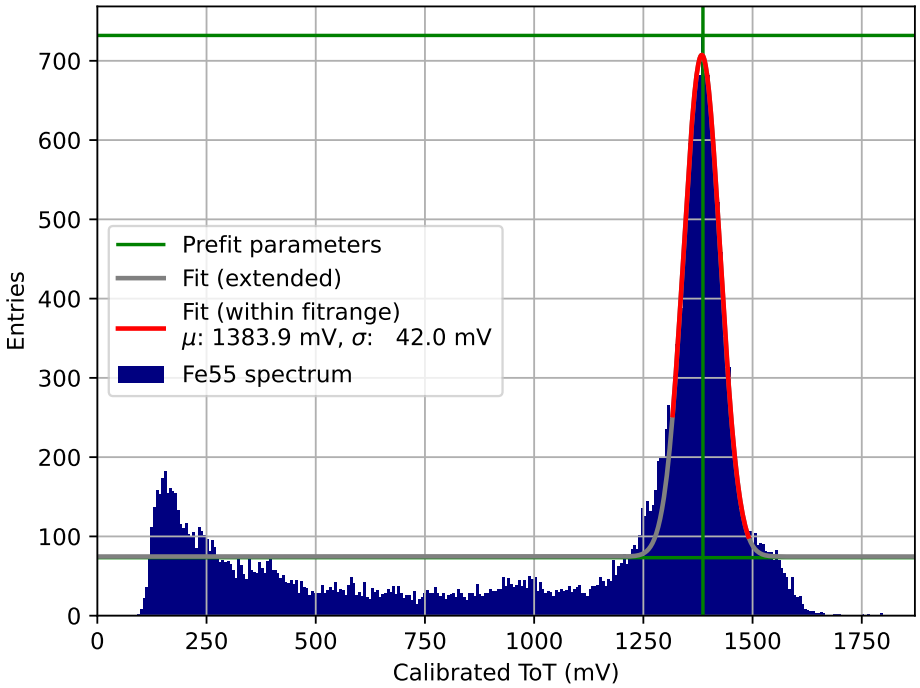


Figure 6.5: Fit applied to the Mn-K$_\alpha$ peak observed in a DPTS. The fit function is a Gaussian plus a constant baseline.

Finally, an energy calibration is performed by using a Gaussian fit of the Mn-K_α peak. An example for this is shown in figure 6.5. The fit function is the sum of a Gaussian and a constant baseline:

$$a \cdot e^{-\frac{(\mathrm{ToT}-\mu)^2}{2\sigma^2}} + b \tag{6.11}$$

a is the peak height above baseline, μ and σ are the peak center and standard deviation and b is the height of the baseline. The literature value of the Mn-K_α is $E_{K_\alpha} = 5.90\,\mathrm{keV}$ [Jun08].

Under the assumption that all of the energy is deposited in the sensor (see section 3.2), a charge of approximately

$$Q_{K_\alpha} = \frac{E_{K_\alpha}}{E_i} \cdot 1\,e = \frac{5.90\,\mathrm{keV}}{3.6\,\mathrm{eV}} \cdot 1\,e \approx 1640\,e \tag{6.12}$$

is deposited by every absorbed K_α-photon. The mean calibrated ToT of the K_α peak should approximate to a charge $ToT_{\mathrm{cal.}}[\mathrm{mV}] \approx Q_{\mathrm{fit}}[e]$ according to equation (6.9) under usage of the nominal injection capacitance C_{inj}. This approximation can be verified by comparing the theoretically deposited charge Q_{K_α} to the reconstructed charge from the K_α fit Q_{fit}. If the approximation is good, both charges should match. It was however found that the deposited charge is usually a bit larger than the charge reconstructed by ToT. The ratio $Q_{K_\alpha}/Q_{\mathrm{fit}}$ is observed to be a factor between 1.0 and 1.2 for various chips and different biasing parameters [Agl+23]. Reasons for this could be that the injection capacitance C_{inj} deviates from its design value of 160 aF [DPT21] or that the effective voltage charging the pulsing capacitor is not exactly V_{h}. Biasing parameters, including the back bias V_{bb}, do not seem to have significant effect on this deviation [Agl+23]. Regardless of the particular reason, a correction factor per chip is introduced to compensate for the deviation of the injected and deposited charge. It is defined as

$$Q_{\mathrm{dep}} = \eta \cdot Q_{\mathrm{ToT}}, \tag{6.13}$$

where Q_{dep} is the charge actually deposited in the sensor and Q_{ToT} is the charge obtained via the calibrated ToT.

Particularly, η is obtained by running a ^{55}Fe source scan on every chip and calculating

$$\eta = \frac{E_{K_\alpha}/E_i}{\mu}, \tag{6.14}$$

where μ is the peak center of the K_α fit in the calibrated ToT spectrum and E_i the mean energy needed to create an electron-hole pair in the silicon lattice. According to this, η would not be dimensionless, but the dimension vanishes, if the approximation equation (6.9) is used. The uncertainty of this factor is obtained by Gaussian error propagation as

$$u(\eta) = \sqrt{\left(\frac{E_{K_\alpha}}{\mu^2}\right)^2 u^2(\mu)}, \tag{6.15}$$

where μ is the center value of the fitted Gaussian function and $u(\mu)$ its fit uncertainty. Using the approximation equation (6.9), it also follows that

$$Q_{\mathrm{dep}}[e] = \eta \cdot V_{\mathrm{h}}[\mathrm{mV}] \tag{6.16}$$

for data from pulsing as well as

$$Q_{\mathrm{dep}}[e] = \eta \cdot \mathrm{ToT}_{\mathrm{cal}}[\mathrm{mV}] \tag{6.17}$$

for data from a source or particle beam in combination with the ToT calibration.

Definition 6.7.1 (Injected charge calibration factor)**.** *An injected charge calibration factor η is introduced to account for deviation between measured and actual injected charge during pulsing of the pixel: $Q_{\mathrm{calibrated}} = \eta \cdot Q_{\mathrm{measured}}$. It is usually obtained via calibration with an ^{55}Fe source.*

6.8 Beam Test Setup and Analysis

Another important observable is the efficiency of the sensor.

Definition 6.8.1 (Efficiency)**.** *The efficiency is the ratio between particles traversing a pixel and actual hits registered at this position in the pixel.*

An ideal sensor would have an efficiency of 100 % while maintaining a negligible fake-hit rate, as these two observables are in a direct trade-off between each other. For the ITS2, an efficiency of 99 % is targeted [Abe+14]. This will also be used as the baseline target efficiency for ITS3 prototypes here. To determine the efficiency of a sensor, it is required to know how many particles were actually traversing the sensor. Therefore, the experimental setup has to be much more sophisticated than for example a ^{55}Fe or a ^{90}Sr source on top of the chip. Other than that, the sensor will be placed in a particle beam and surrounded by well-characterized reference planes to identify particle tracks through the sensor plane. A detailed description of the setup used in beam tests is attached in appendix A.

Results from beam tests are analysed with *Corryvreckan* [KSW19]. This framework enables the reconstruction of tracks through the telescope planes, which is necessary to calculate the sensor efficiency. Furthermore, there are modules to calculate the spatial and temporal resolution of the sensors. In particular, *Corryvreckan* will fit tracks through clusters in the ALPIDE planes, using the General Broken Lines Algorithm [Blo06]. Recorded events are only considered good if there is only one track in this event, if $\chi^2 < 3$ is satisfied for this track *and* if there has been a hit on every reference plane. Furthermore, tracks crossing

the DUT in the outermost 2 pixels (30 µm) will be rejected. Lastly, pixel with a fake-hit rate larger than 1000 times the average fake-hit rate were masked in analysis. Cluster on the DUT are then associated with an accepted track, if track traverses the DUT in a circle of 480 µm radius around the hit on the DUT plane. This is done because hits with failing decoding will be assigned to the pixel (c=15, r=15) in the middle of the matrix. In order not to underestimate the efficiency because of failing decodings, such a loose association window is chosen. To keep the probability of assigning the track to a fake-hit low, a time association window of 1.5 µs is chosen.

7 Ionizing Radiation

This chapter summarizes the studies that were done to study ionization damage from ionizing radiation. X-rays are used here, because unlike for example protons, low energy X-rays do not create displacement damages at the same time. The threshold energy for displacement damage from X-rays is 250 keV, so far higher than the X-rays used here. [Spi05] It is therefore possible to disentangle ionization and displacement damage. In view of the ITS3 project, it is important to prove the radiation hardness of the *TPSCo.* 65 nm CMOS technology and this specific sensor implementation up to radiation doses of 10 kGy [Agl+23]. Furthermore, this study can be used to scope the radiation hardness looking forward to the ALICE 3 Vertex Detector. As of writing, it is estimated to be roughly 3 MGy. This is calculated by the expected dose rate per month of 58 kGy/month [Col22a, Table 1] and a rough estimate of 50 months of active accelerators during LHC run 5 and 6 with approximately 2/3 of up time over the year.

7.1 Setup

In two separate campaigns, chips were irradiated with 10 MeV X-rays from a tungsten target at CERN. The first campaign was carried out in July 2022 and the second one in March 2023 Although the two campaigns were carried out in two separate X-ray machines, the results are comparable because the machines are regularly calibrated. The amount of ionizing radiation is quantified as Total Ionizing Dose (TID).

It is foreseen to run a quick threshold scan over parts of the matrix, as well as a fake-hit rate scan after every irradiation step. Furthermore, all the chip currents I_a, I_d, I_b and I_{VBB} are monitored, especially during the irradiation steps themselves. The setup from July 2022 uses the DPTS breakout board, where the voltages for the analog, digital and CML buffer power domains are supplied separately by different power supply channels to the chip. All currents are measured by reading values from the power supply via USB. In March 2023, a setup with proximity and DAQ board is used. This way, the power domains are supplied by voltage regulators on the DAQ board. There are current monitors for these power domains on the DAQ board, which are read out during the irradiation periods.

The ambient temperature in the X-ray machine is monitored by a pressure-temperature-humidity (PTH) probe, fixed close to the carrier PCB but out of the X-ray beam itself. During the March 2023 campaign, temperatures up to 32 °C were measured in the machine. It is known that the threshold and fake-hit rate of a chip are temperature-dependent (see also section 8.2 and [Agl+23]). After finishing the irradiation of the first three chips, it was therefore decided to install a cooling jig to the setup to lower, and more importantly to stabilize the chip temperature. The back side of the carrier PCB is cooled down to 20 °C. The temperature of the cooling jig is then also monitored by a temperature probe. After the end of the irradiation, the fake-hit rate and threshold of the chips is monitored closely with increasing intervals as the time passes on. An analysis of the S-curve noise is not done here, as it was found that already moderate fake-hit rate make the S-curve noise calculation very inaccurate. This is discussed in detail in appendix B. The same effect could potentially also influence the threshold measurement, but the magnitude of this effect is much lower there.

A total of five chips has been irradiated in an irradiation campaign in July 2022. An overview about all chips with their doses and rates is given in table 7.1. After irradiation, the chips are stored in a freezer at −20 °C, with the exception of short periods of measurement.

Table 7.1: Overview of all chips from the July 2022 TID irradiation campaign. All chips were unirradiated prior to the campaign.

Chip ID	Total Dose	Dose Rate	Comment
DPTSXW22B8	100 kGy	$1\,\mathrm{kGy\,min^{-1}}$	
DPTSSW22B21	10 kGy	$1\,\mathrm{kGy\,min^{-1}}$	Damaged wire bonds
DPTSSW22B22	500 kGy	$1\,\mathrm{kGy\,min^{-1}}$	
DPTSOW22B23	100 kGy	$0.12\,\mathrm{kGy\,min^{-1}}$	Draws current above limit
DPTSXW22B26	10 kGy	$1\,\mathrm{kGy\,min^{-1}}$	

In the campaign of March 2023, 7 chips were irradiated, of which one is the same as in July 2022. Table 7.2 gives an overview of all DPTS that have been irradiated in this campaign. Having learned from the challenges occurring in the July 2022 campaign, the objectives are set slightly different here. To rule out chip-to-chip variation effects, every irradiation is performed twice with separate chips, except for the 5000 kGy due to lack of time. The dose rate is fixed to $1\,\mathrm{kGy\,min^{-1}}$ as aspects other than differing dose rates are prioritized here. This exact value is chosen because it is close to the maximum, the X-ray machine can achieve, which reduces the time needed. Furthermore, all chips used here are characterized in all possible aspects in the lab prior to irradiation. This includes a fake-hit rate scan, a threshold and ToA scan on the whole pixel matrix, decoding calibrations and a ^{55}Fe source scan. It was decided to store the chips at ambient temperature (20 °C) in the lab after the irradiation to simulate an environment as it is foreseen for the ITS3.

The standard settings for irradiated chips are also applied here. That means increasing I_{reset} from 10 pA to 35 pA and decreasing I_{db} from 100 nA to 50 nA. With exception of the operation during the in-beam test, the chips at levels of 10 kGy and 100 kGy are operated at $V_{\text{bb}} = -1.2\,\text{V}$. As usual, V_{casn} at this back bias is set to 250 mV. At higher dose levels, $V_{\text{bb}} = -3.0\,\text{V}$ is chosen. This is done to receive a larger operational margin at higher dose levels, such that the back bias does not have to be changed during the studies. The other parameters are the default values reported in table 6.1. Chips with threshold tuning intended are tuned to a mean threshold of $125\,e$. Furthermore, chips where a threshold drop should be observed are initially tuned to $350\,e$. Lastly, it has to be noted that the thresholds reported in this chapter are *not* corrected by the injected charge calibration factor η, as by the time of taking data for these measurements, it was not yet fully understood, if and how such corrections have to be applied. Future measurement campaigns should consider this to render the results more comprehensively. The only exception is the section about efficiencies (cf. section 7.8), as no threshold tuning was done there and injected charge calibration factors of these chips are known.

Table 7.2: Overview of all chips from the March 2023 TID irradiation campaign in chronological order of their irradiation. The dose rate was $1\,\text{kGy}\,\text{min}^{-1}$ in all cases.

Chip ID	Total Dose Before	Total Dose After	V_{casb}	Temperature Control
DPTSSW22B22	500 kGy	1000 kGy	Tuned	None
DPTSOW22B43	0 kGy	100 kGy	Tuned	None
DPTSOW22B42	0 kGy	100 kGy	Tuned	None
DPTSOW22B45	0 kGy	10 kGy	Tuned	20 °C
DPTSOW22B47	0 kGy	10 kGy	Tuned	20 °C
DPTSOW22B46	0 kGy	500 kGy	Constant	20 °C
DPTSOW22B44	0 kGy	500 kGy	Constant	20 °C
DPTSSW22B22	1000 kGy	5000 kGy	Constant	20 °C

7.2 Chip Current Measurements

Out of the five chips that were irradiated with X-rays in July 2022, three are still functional. The chip with the ID DPTSOW22B23 shows strongly rising currents during irradiation. The current measurement of this chip is shown in figure 7.1. In the beginning, the current of the digital power domain I_d (cf. figure 5.4, I_d powers the digital domain in the pixel, as well as shift register, hit merger and CML driver in the periphery) decreases from initial 1.7 mA to about 1.4 mA, like it is observed in many other TID-irradiated chips. About 4 hours into irradiation, the current suddenly starts to rise up to 3.5 mA in the next 7 hours. Next, a sudden jump occurs and I_d is now about 6.3 mA, but without rising further until the end of

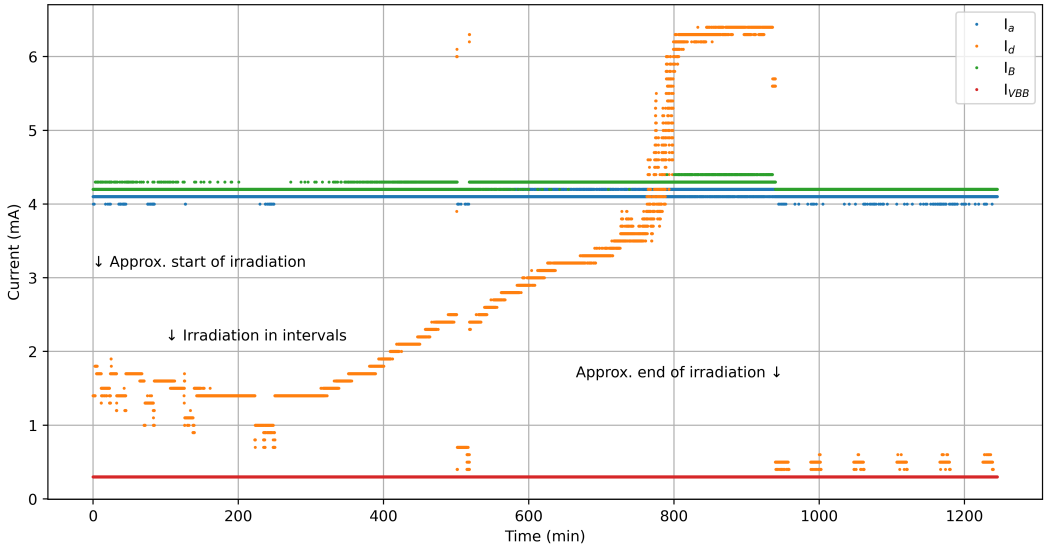


Figure 7.1: Current measurement of DPTSOW22B23 during irradiation with X-Rays. The time is relative to the start of the first current measurement.

the irradiation. When the irradiation finishes, the current drops down to 0.5 mA. The chip monitoring ends about 20 hours after beginning of irradiation. When trying to power on the chip about a month after the end of the irradiation, it is found that the digital current is about $I_d \approx 19\,\text{mA}$, being much higher than in every other known working chip. A shift register test fails. No further tests on this chip are done as operation with unexpected shift-register behavior will render any results unreliable. It is worth mentioning here that the shift register is powered by the digital power domain with the current I_d. It is therefore possible that the shift register itself experienced a severe damage due to ionizing radiation. It can not be excluded that this behavior is not a direct consequence of irradiation but rather the consequence of having chosen a bad chip. This theory is supported by the fact that there is at least one more chip with permanently failing shift register tests from the beginning on as well as that there are in total 6 more TID-irradiated chips with equal or higher dose that do not show such problems. As this chip is the only chip being irradiated at a lower dose rate, no studies on the effects of dose rate can be carried out within the scope of this thesis. For future measurement campaigns, this will be another aspect to be studied, as the dose rate in laboratory tests is naturally orders of magnitude higher than the dose rate in the actual ALICE ITS will be later on. It would therefore be interesting if and how results from this chapter change, when the dose rate is varied.

Figure 7.2 shows the current measurement of DPTSXW22B8. This chip received a total dose of 100 kGy. It can clearly be observed that the supply current of the digital power domain I_d decreases with increasing irradiation dose level. It starts off at about 1.2 mA, dropping down to about 0.3 mA at higher dose levels. The analog power domain current I_a and the

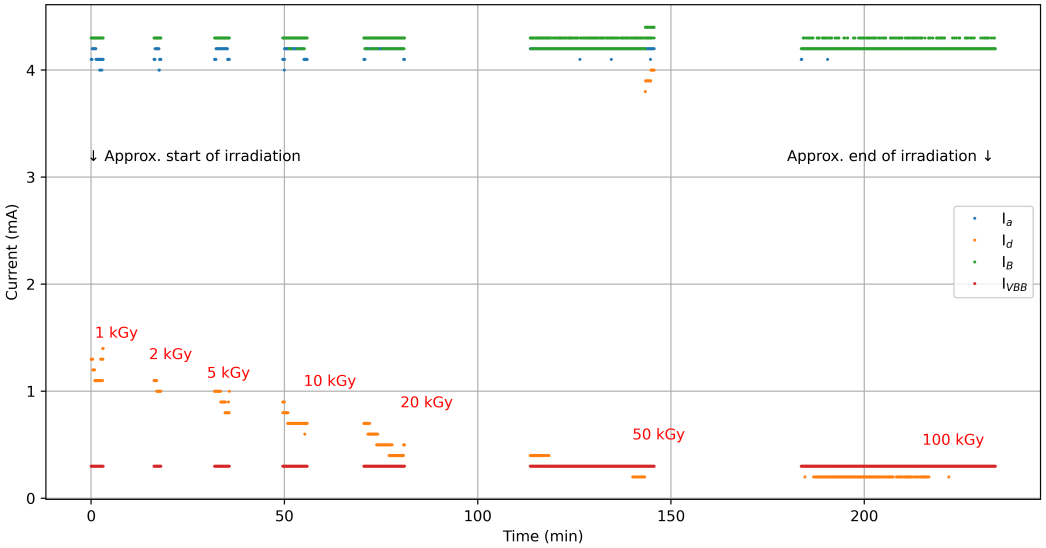


Figure 7.2: Current measurement of DPTSXW22B8 during irradiation with X-Rays. The time is relative to the start of the first current measurement.

CML buffer current I_b, as well as the current towards the back bias in the PWELL and SUB domains I_{VBB} are constant and therefore unaffected by irradiation at these dose levels.

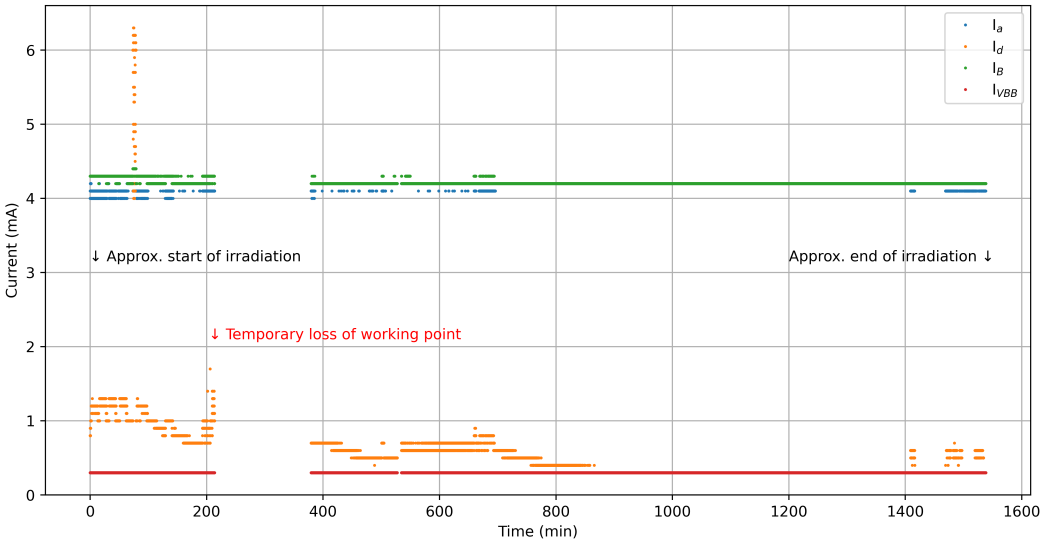


Figure 7.3: Current measurement of DPTSXW22B22 during irradiation with X-Rays. The time is relative to the start of the first current measurement.

In figure 7.3, the current measurement of DPTSXW22B22 can be seen. Here, the current I_d shows a short spike from the baseline of 1.1 mA up to 6.3 mA about 1 hour into irradiation. It disappears without any obvious consequences. This behavior is not yet understood. About 3.5 hours into irradiation, the working point of the chip is lost temporarily. Shortly before, I_d began to rise up to 1.8 mA. After another 3 hours, the chip begins to work again normally,

with the known general drop of I_d. The other current measurements of the March campaign show no unexpected behavior and can be found in the appendix in figures C.1 and C.2.

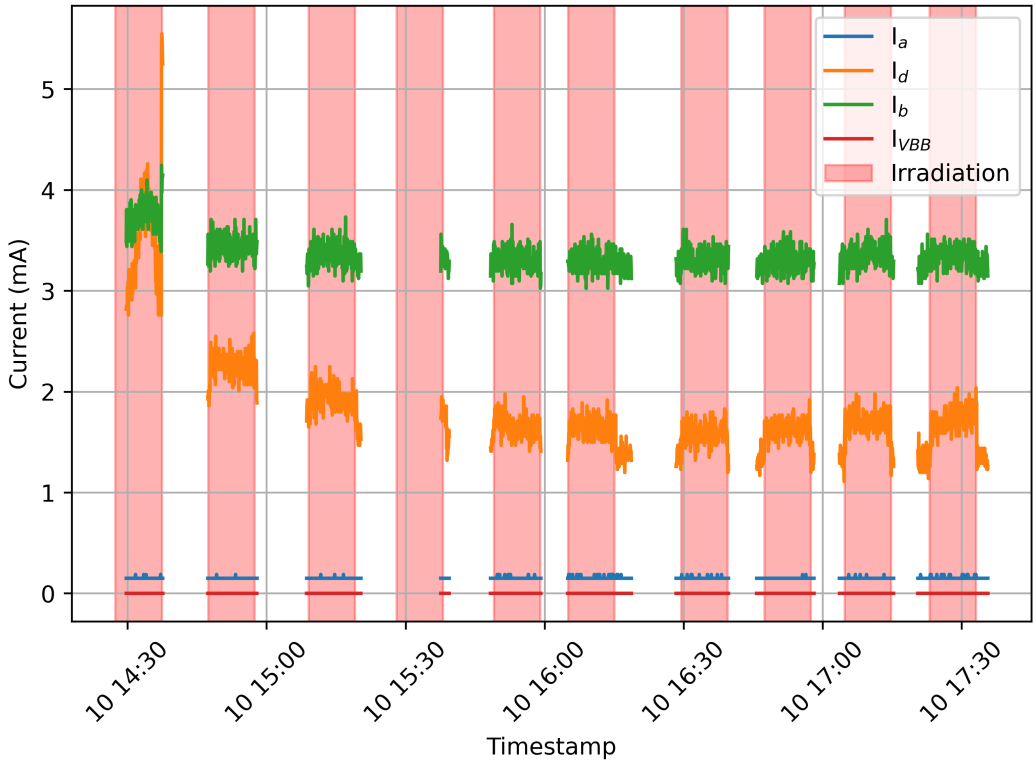


Figure 7.4: Current measurement of DPTSOW22B42 during irradiation with X-Rays.

The current measurement of DPTSOW22B42 is shown in figure 7.4. In the March 2023 irradiation campaign, exact timestamps of times with and without irradiation are available. There is, however, no current measurement during most of the time in between the irradiation steps. This is because the currents are measured by ADCs on the DAQ board rather than by the power supply itself. It is a consequence of not using the DPTS breakout board, but the setup with proximity and DAQ board which prevents easy current readings during the operation of the chip, to take for example threshold or fake-hit rate scans. The shown chip received a total ionizing dose of 100 kGy. It is again clearly observable that the digital domain current I_d decreases with increasing irradiation level.

With the information on irradiation times, it can also be seen that I_d increases by about 0.5 mA in times, where the X-ray machine is switched on, while dropping back to the regular level immediately afterwards. This can be explained by high hit activity in the chip due to incoming X-rays. Certain parts of the circuitry in the digital power domain are only active after an incoming hit. Thus, a high hit rate increases the current in this domain temporarily. The same goes for the analog power domain, where for example the current I_{db} is only flowing when the pixel is asserted or deasserted, as well as for the CML buffer domain. A temporary

increase of these currents can be observed, although the effect is much smaller than for the I_d current. Furthermore, it is observed that the CML buffer current I_b is showing a falling trend with increasing irradiation levels. The baseline of I_b in the beginning of the irradiation is about 3.6 mA dropping down by 0.4 mA to about 3.2 mA. The reason for this current drop is not yet understood and would require more detailed simulations and studies.

The current measurements of the other chips show no previously unknown features and can be found in the appendix figures C.3 to C.7. After all, the sudden current spikes, losses of operating points and the drop of several chip currents is not yet understood and would need further studies. However, since the current measurements from the March 2023 irradiation campaign do not show special features, except for drop in some supply currents, it can be assumed that these chips work sufficiently well during and after irradiation.

7.3 Threshold

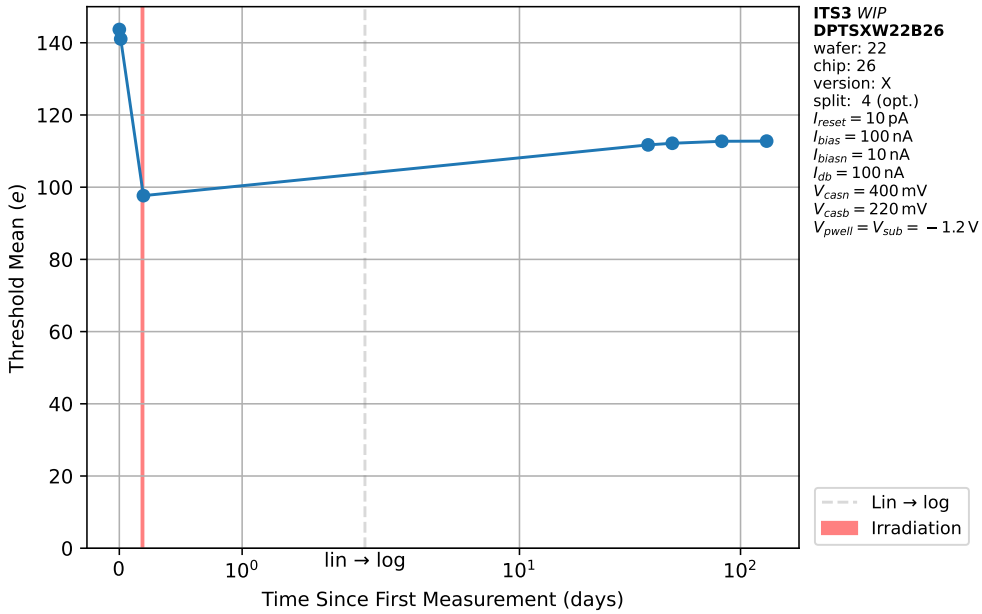


Figure 7.5: Threshold mean vs. time for a sensor exposed to 10 kGy of ionizing radiation.

Figure 7.5 shows the evolution of the mean threshold of a chip during and after receiving a ionizing dose of 10 kGy. Before the irradiation, the mean threshold of this chip at this operating point is about 140 e. The irradiation makes the threshold drop to about 100 e. 48 d after end of the irradiation, the mean threshold recovers by about 10 e up back to 110 e. During this time, the chip is stored mostly at $-20\,°C$, with exception of some short ($\mathcal{O}(1\,d)$) periods, where the chip is being measured at the temperature in the laboratory of

about +20 °C. This data gives a first glimpse of the general behavior of the threshold under influence of ionizing radiation. Further analysis regarding the threshold evolution of chips from July 2022 is not done here, as the chip operating point was not kept constant over time during irradiation as well as during annealing. Thus, this chapter will focus only on the data from March 2023, where these challenges were identified, enabling the study of different aspects as in July 2022.

7.3.1 Constant Biasing Parameters

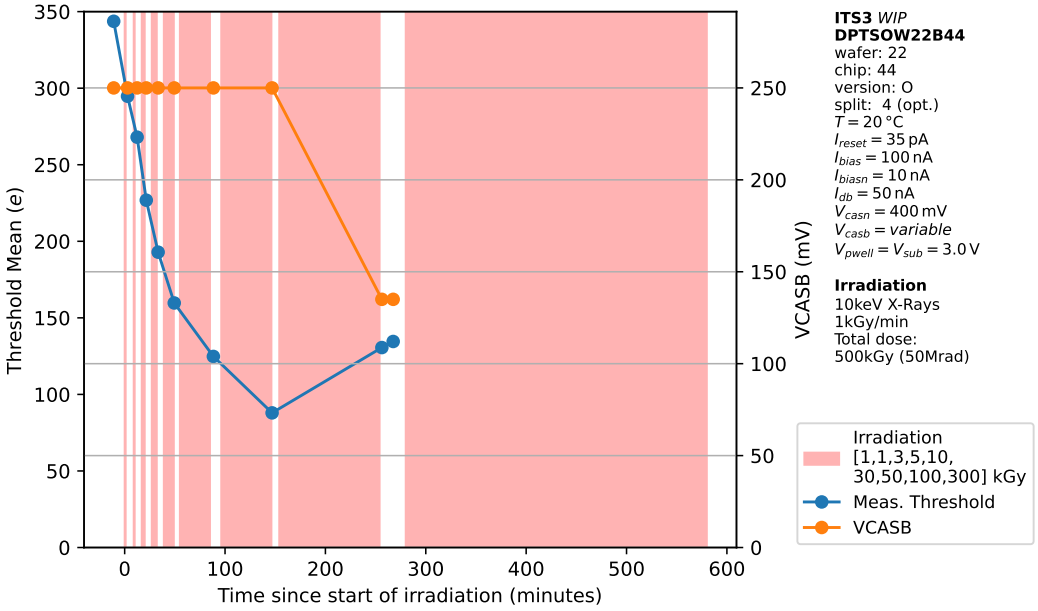


Figure 7.6: Mean threshold and V_{casb} vs. time for a chip with a total dose 500 kGy. V_{casb} had to be tuned after 200 kGy in order to keep the chip operational. The chip was not operational immediately after the total dose of 500 kGy.

Figure 7.6 shows the evolution of the threshold over time for a chip that has been irradiated up to 500 kGy. It is needed to adjust the operating point after a dose of 200 kGy because the threshold scans were failing otherwise. Directly after 500 kGy, the chip is not operational at all. Similar observations have been made for the other chip at this level in the appendix figure C.8. Data from both chips are combined in figure 7.7. It is visible that the mean threshold of both sensors drops down as the radiation dose increases. Furthermore, it is observable that during the first irradiation steps, the decrease in threshold is much stronger. This shows that ionizing radiation damage is not a linear process, but rather exponential. The first kGy of ionizing radiation dose causes more damage than later on. The threshold degradation of the sensor is strongest right after beginning of the irradiation. After 100 kGy, the threshold of one chip decreased from the initial 344 e down to 88 e, effectively reducing

the mean threshold of the sensor by 256 e. The other chip threshold is reduced from 327 e to 87 e, giving a reduction of 240 e.

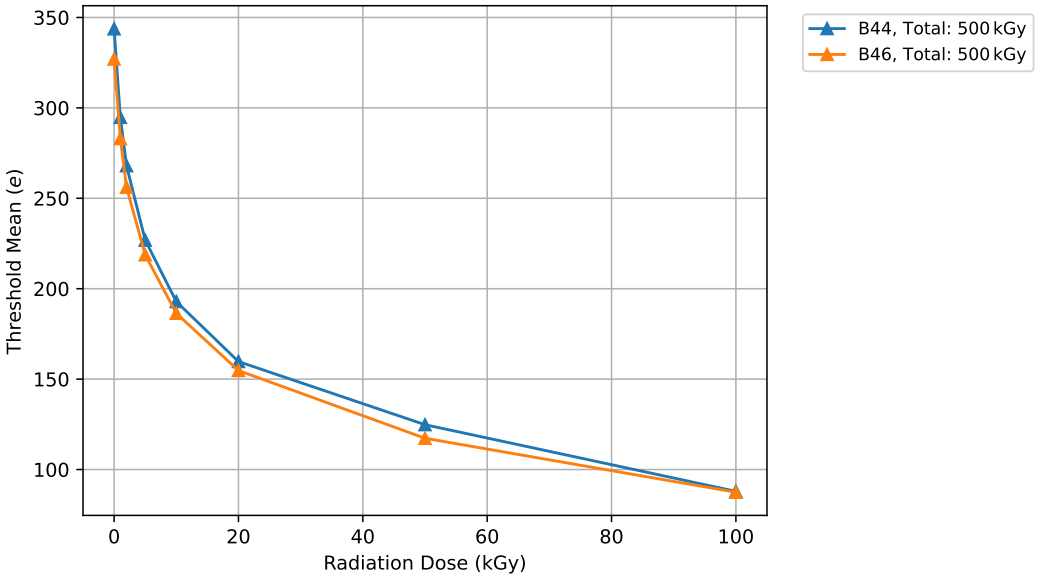


Figure 7.7: Threshold mean vs. radiation dose for the two chips that have been irradiated without tuning the threshold. The data is cut at 100 kGy to exclude data taken with different V_{casb}.

7.3.2 Tuning for Constant Threshold

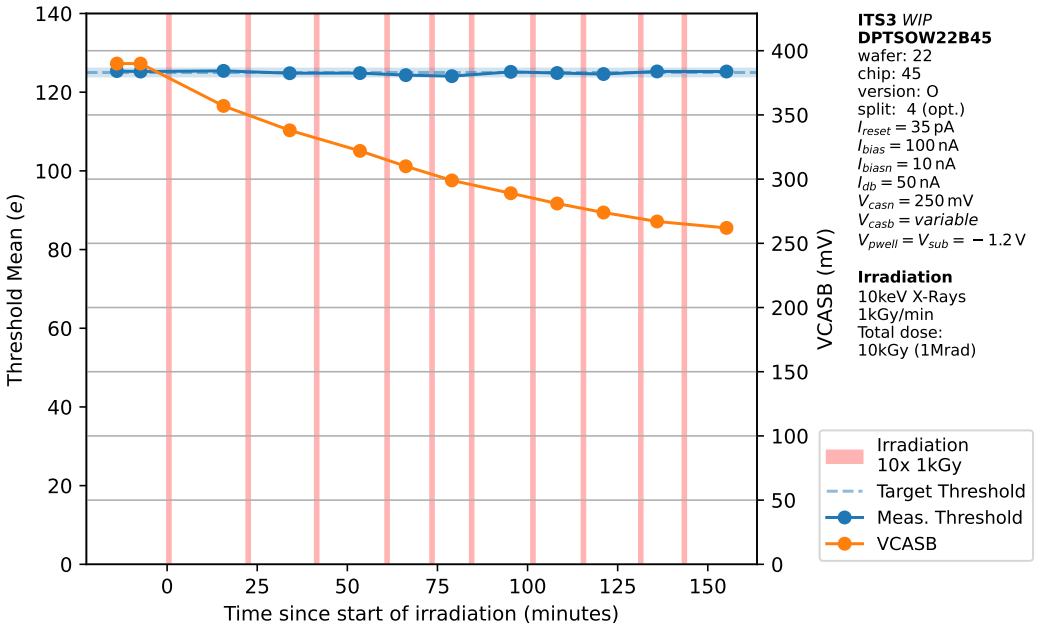


Figure 7.8: Mean threshold and V_{casb} vs. time for a chip with a total dose 10 kGy. The threshold is tuned back to 125 e after every irradiation step.

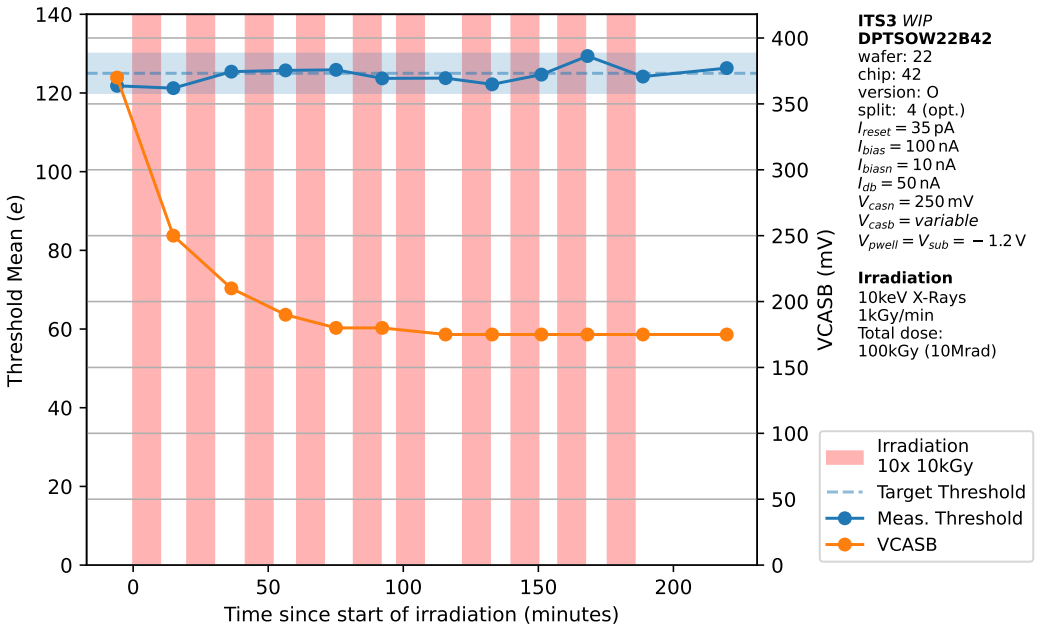


Figure 7.9: Mean threshold and V_{casb} vs. time for a chip with a total dose 100 kGy. The threshold is tuned back to 125 e after every irradiation step.

Another study was done with four other chips. Here, the operating point is initially tuned to 125 e. Then after each radiation step, the threshold is tuned back to the original value with a margin of $\pm 2\,e$ for 10 kGy chips and $\pm 5\,e$ for 100 kGy. This is done by adjusting V_{casb}. Figure 7.8 shows the evolution of V_{casb} over time for a chip which received a total dose of 10 kGy. One irradiation step equals 1 kGy of ionizing dose. Over the total 10 kGy, V_{casb} has to be lowered by 28 mV in order to keep the threshold constant, where larger adjustments had to be made after the first irradiation steps than later on at higher doses. In figure 7.9, the same curve for one of the 100 kGy chips is shown. V_{casb} has to be lowered by 195 mV here.

The respective plots for the other both chips can be seen in the appendix figures C.9 and C.10. It is known from other measurements that annealing can have quite severe effects in the first minutes after the end of irradiation. A possible hypothesis for the saturation of the V_{casb} after about 60 kGy is that here the threshold drop after an irradiation step is compensated for by the annealing within the time between end of irradiation and start of the threshold scan. Furthermore, even during irradiation, annealing effects could already occur. To verify this hypothesis, a measurement program with variable dose rate could be done. If the dose rate is significantly lower (i.e. 0.1 kGy min^{-1} instead of 1 kGy min^{-1}), the average time between the creation of one particular defect and the threshold scan would be larger, giving statistically more time for the defect to anneal. Therefore, it would be expected that overall, smaller

adjustments of V_{casb} are necessary and V_{casb} in the equilibrium has a higher value than at a higher rate.

The plot in figure 7.10 shows the evolution of V_{casb} of all four chips combined. The y-axis is normalized by the first measurement at zero radiation dose in order to keep the measurements more comparable. The x-axis is normalized by the accumulated dose instead of time. This introduces some uncertainty, because the intervals between irradiation steps are not necessarily equally long, especially when comparing 10 kGy to 100 kGy chips. As mentioned before, a different time difference between these measurements could render the measured threshold incomparable because there was another time span, in which annealing effects could have occurred. At the chosen dose intervals all chips have had an intermediate dose of 10 kGy at some point. For the 10 kGy chips, this is obviously after the last irradiation step, so roughly 2.5 h after beginning of the first step. For the 100 kGy chips, this dose is reached after the first irradiation step, which corresponds to about 15 min after beginning of the first step. Thus, the chips at high rate have much less time for intermediate annealing processes to recover the threshold. If these intermediate processes play a significant role, one would expect to see the data points of 100 kGy chips after 10 kGy at a lower V_{casb} value than the data points for the 10 kGy chips. The plot shows no such behavior. In fact, the curves of B43 (10 kGy) and the two 100 kGy match within $2\,e$. Just the measurement of B42 deviates by $8\,e$ from this. However, this could be explained by the fact that the threshold for B42 at this point is not tuned optimally, as seen in figure 7.9. With $121\,e$, this is rather close to the lower edge of the accepted margin. As an increase of V_{casb} generally leads to a decrease of the threshold, a more precisely tuned V_{casb} would lay some mV lower, so in a region compatible with the other chips.

After a cumulated dose of 70 kGy, against the general trend, V_{casb} is increased to stabilize the threshold for the B43 chip. The measured threshold is at the lower end of the accepted margin of $(120 \pm 5)\,e$. Since increasing V_{casb} leads to a decrease of threshold, the target threshold potentially could have been reached more precisely with a lower V_{casb} value. The margin of $\pm 5\,e$ was rather arbitrary and just chosen higher for the 100 kGy steps in order to save some time on tuning. It became clear that the tuning takes a lot less time than expected. For future irradiation campaigns, it could therefore be considered to decrease the margin to $\pm 2\,e$ or even further in order to have more consistent data on the V_{casb} evolution. The other chip at these doses did not show such behavior. The value of V_{casb} remained unchanged after 60 kGy. Some fluctuation within the margin of the threshold can be observed, but no clear trend is identified. As for the threshold it can be concluded that under these operating conditions, the margin of V_{casb} alone is enough to maintain a tuned threshold while irradiating the sensors up to 100 kGy, which is 10 times above the requirements needed for the ITS3 [Agl+23].

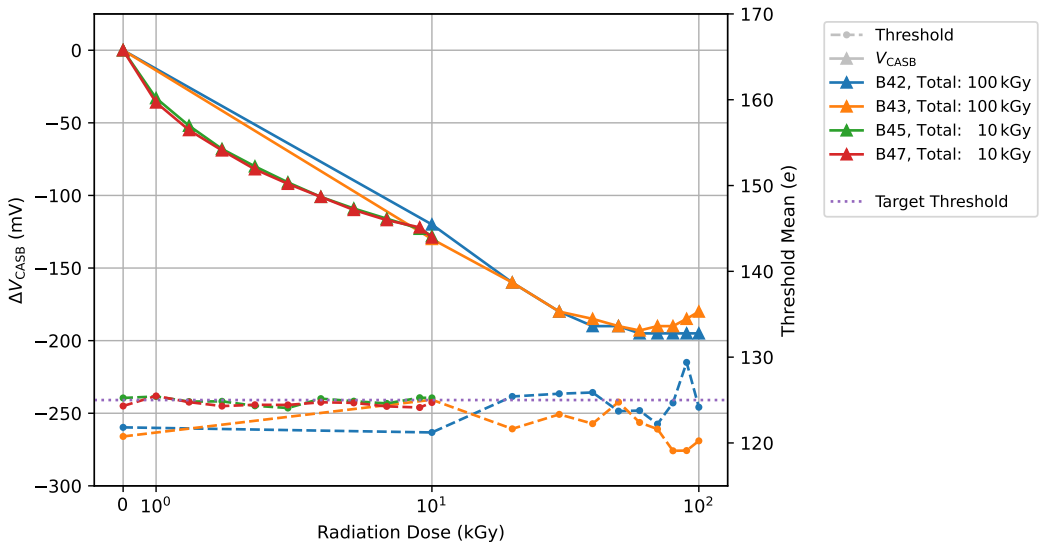


Figure 7.10: V_{casb} and mean threshold vs. radiation dose for four different chips. The threshold is tuned back to 125 e after every irradiation step.

7.4 Fake-Hit Rate

In measurements of irradiated sensors from July 2022, it is nicely visible that exposure to ionizing radiation leads to an increase of fake-hit rate in the sensors. This section will study the effects of ionizing radiation on the fake-hit rate under the two already known operation schemes: Constant biasing parameters and threshold-tuned operation.

7.4.1 Constant Biasing Parameters

In figure 7.11, the evolution of the fake-hit rate for chip B44 is depicted. Up to a radiation dose of 20 kGy, the fake-hit rate stays at the lower sensitivity limit when keeping the biasing parameters constant. After 100 kGy, the fake-hit rate rises to $(101\ ^{+96}_{-71})\cdot 10^2\,\text{pixel}^{-1}\,\text{s}^{-1}$. After another 100 kGy, so at a total dose of 200 kGy, the chip is not immediately operable with unchanged biasing parameters. Probably, the ionizing radiation damage lowers the threshold so strongly that no more stable operation is achievable. To overcome this, V_{casb} is lowered from 250 mV to 135 mV, which makes the chip operable but renders the results on fake-hit rate not directly comparable. In the first minutes after the end of the last irradiation step towards the total dose of 500 kGy, the chip is completely unresponsive, so that no further data points are collected here. The other chip with exponential steps to 500 kGy, B46, shows comparable results. The only difference there is that the chip is monitored for a while longer after the end of irradiation and thus, some data points at full dose exit. These are, however, at tuned V_{casb}. The trend can be seen in figure C.11. In conclusion, if the chip biases are not tuned, the fake-hit rate starts rising at a dose of 20 kGy, while reaching the maximum of this

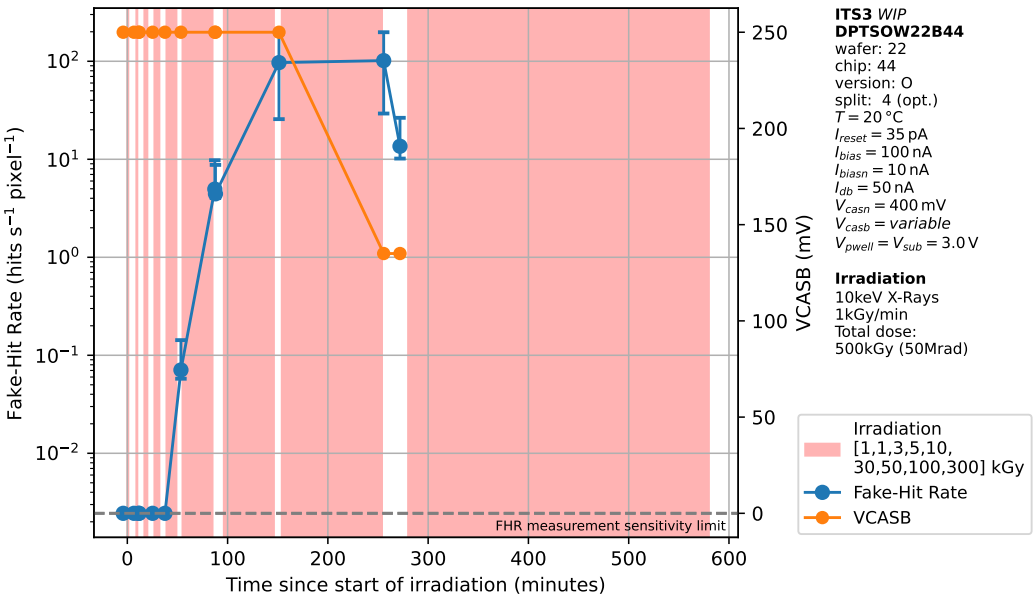


Figure 7.11: Fake-hit rate and V_{casb} vs. time for a chip with a total dose 10 kGy. After 200 kGy, V_{casb} had to be tuned to keep the chip operational. Immediately after 500 kGy, the chip was unresponsive.

particular measurement procedure at about 200 kGy. Figure 7.12 shows the fake-hit rate in dependency of the radiation dose for those two chips. It is observable that the fake-hit rate of the B44 is rising at lower doses than the fake-hit rate of the B46 chip. This can likely be attributed to chip-to-chip variations.

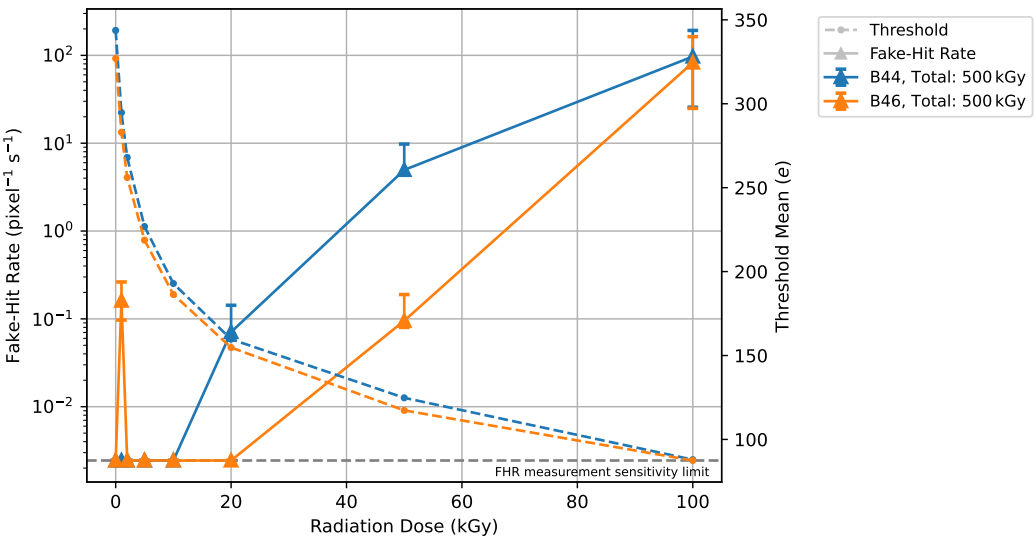


Figure 7.12: Threshold mean and fake-hit rate vs. radiation dose for two chips irradiated to 500 kGy. The biasing parameters are kept constant over all doses.

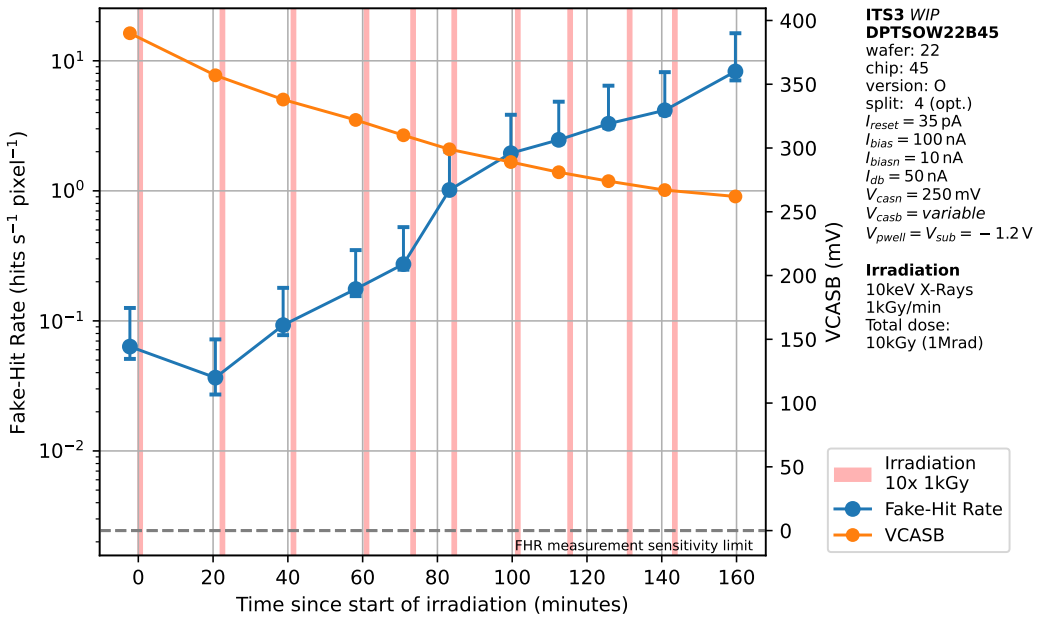


Figure 7.13: Fake-hit rate and V_{casb} vs. time for a chip with a total dose 10 kGy. The threshold is tuned back to 125 e after every irradiation step.

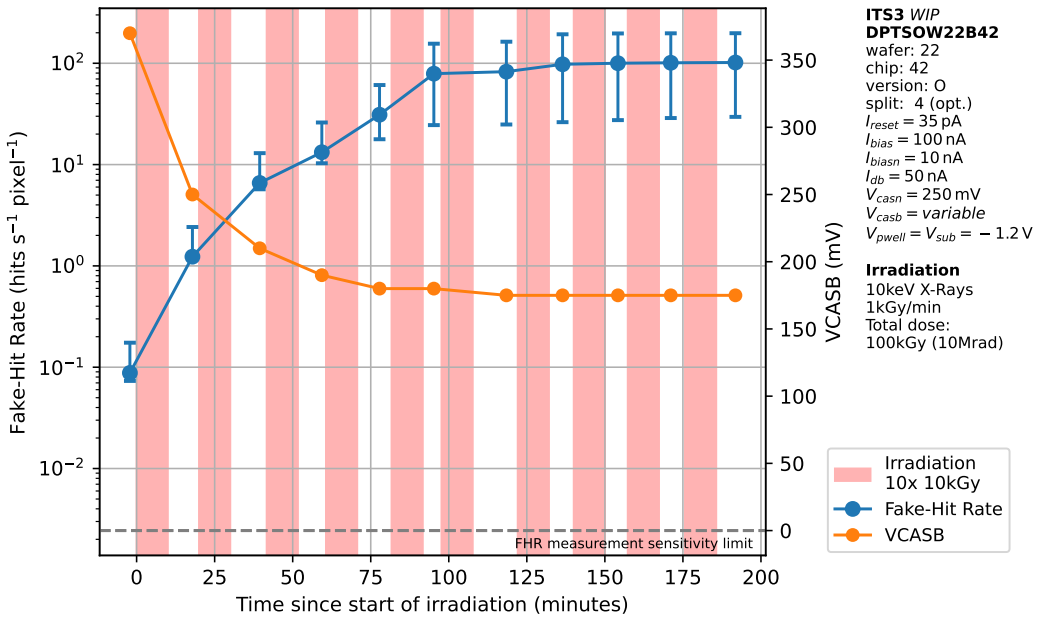


Figure 7.14: Fake-hit rate and V_{casb} vs. time for a chip with a total dose 10 kGy. The threshold is tuned back to 125 e after every irradiation step.

7.4.2 Tuning for Constant Threshold

Figure 7.13 shows the evolution of fake-hit rates over time. With exception of the fake-hit rate scan after the first irradiation dose, the fake-hit rate increases monotonously with increasing irradiation dose. However, the data points before and after the first irradiation step fall within 1σ with respect to each other. At the beginning of irradiation, the fake-hit rate was $(6.34\ ^{+6.23}_{-1.24}) \cdot 10^{-2}\,\mathrm{pixel}^{-1}\,\mathrm{s}^{-1}$. This is already quite high for a chip tuned to $125\,e$. Many other chips at this operating point have a fake-hit rate lower than or equal to the sensitivity limit. During the irradiation, the fake-hit rate increases exponentially up to a maximum of $(8.29\ ^{+8.00}_{-1.21})\ \mathrm{pixel}^{-1}\,\mathrm{s}^{-1}$. The fake-hit rate increases by approximately two orders of magnitude. However, even if it was quite high from the beginning on, it is still under the limit of $10\,\mathrm{pixel}^{-1}\,\mathrm{s}^{-1}$, which is considered to be the maximum acceptable fake-hit rate during beam tests. Therefore, it would have been possible to study the efficiency in beam immediately after the end of irradiation. This was not done here, but it would be a further useful study for the future. Figure 7.14 shows the evolution of one chip that received a total dose of 100 kGy. Without any dose added, this chip has a fake-hit rate of $(8.28\ ^{+8.01}_{-1.21}) \cdot 10^{-2}\,\mathrm{pixel}^{-1}\,\mathrm{s}^{-1}$, which is comparable to the chip with the lower dose mentioned before. After 70 kGy, the fake-hit rate saturates at about $(97.7\ ^{+95.5}_{-72.6}) \cdot 10^{2}\,\mathrm{pixel}^{-1}\,\mathrm{s}^{-1}$. This saturation is not comparable to the saturation of the threshold, as here, it is only due to limitations of the data taking script (cf. section 6.4). For future measurements, it would be desirable to increase this limit, although at the cost of increased data size to store.

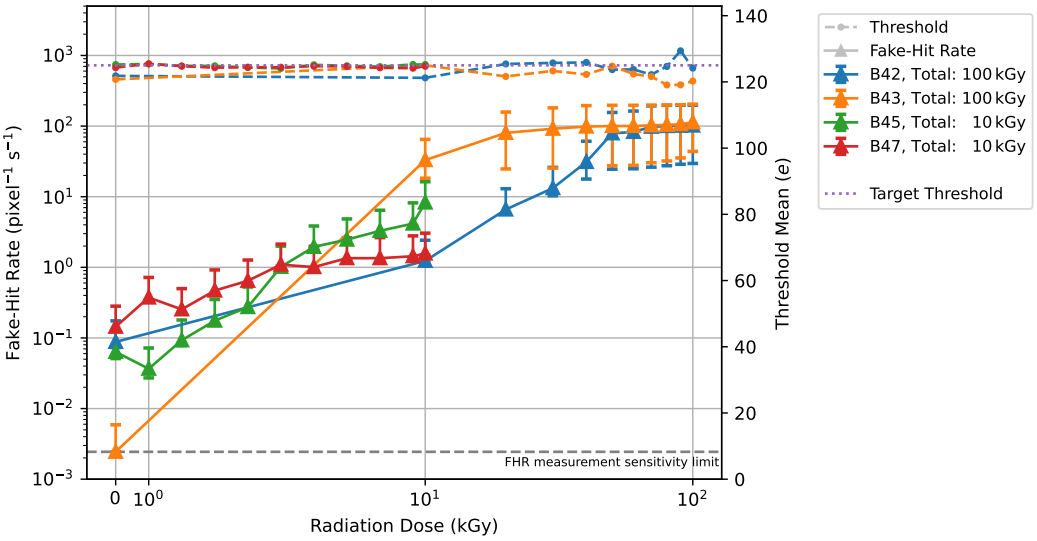


Figure 7.15: Fake-hit rate and mean threshold vs. radiation dose for four different chips. The threshold is tuned back to $125\,e$ after every irradiation step.

The full overview over the four chips that were threshold-tuned is given in figure 7.15. It shows the fake-hit rate in dependency of the ionizing radiation dose. It is visible that the sensor B43

is the only one that has a fake-hit rate around the lower measurement sensitivity limit at the start of the irradiation. However, after its first irradiation step of 10 kGy, this sensor is the noisiest of all samples with a fake-hit rate of $(3.30\ ^{+3.18}_{-1.47}) \cdot 10^1\ \mathrm{pixel}^{-1}\,\mathrm{s}^{-1}$. This is more than 4 times higher than the second noisiest chip B45 with a fake-hit rate of $(8.28\ ^{+8.01}_{-1.21})\ \mathrm{pixel}^{-1}\,\mathrm{s}^{-1}$. Since the required change in V_{casb} is comparable over all chips at this radiation step, it can thus be assumed that not all chips react in the same way to effects of ionizing radiation, but that there is also a certain degree of radiation-dependent chip-to-chip variation. It is again visible that the fake-hit rate reaches the upper sensitivity limit for both of the chips that were irradiated up to 100 kGy. The benchmark of $10\,\mathrm{pixel}^{-1}\,\mathrm{s}^{-1}$ for usage of data in beam tests was exceeded already in the first irradiation step. Both 10 kGy and the other 100 kGy chip fall under this limit. The latter exceeds this value after the 30 kGy irradiation step.

7.5 Studies on Sensors with Higher X-Ray Doses

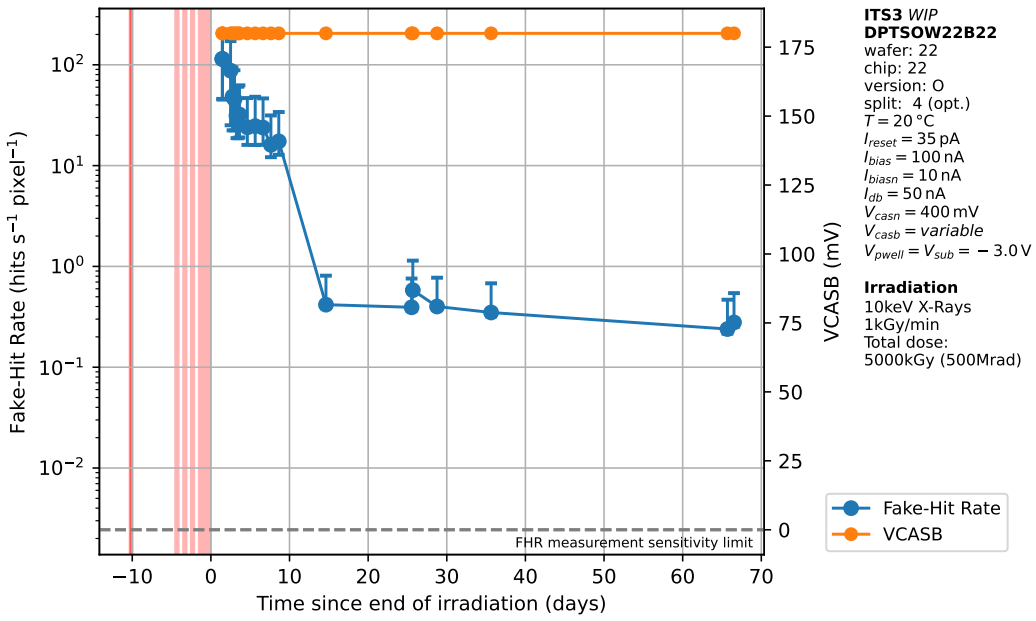


Figure 7.16: Fake-hit rate vs. time for a DPTS with a total dose of 5000 kGy. Tables 7.1 and 7.2 show the exact schedule of irradiation.

The chip DPTSSW22B22 is, up to now, the only chip that has been irradiated multiple times. This is especially interesting because the total radiation dose could be pushed to 5 MGy in the last step of irradiation. This radiation dose lies in the magnitude of what will be required for the ALICE 3 Vertex Detector, which is estimated to roughly 3 MGy, as of writing this thesis. Immediately after irradiation, the chip is completely unresponsive and even after power cycling, no response in the CML outputs can be observed. Then after approximately 8 hours after the end of irradiation, activity on the CML outputs can be observed. However,

the fake-hit rate is so high that the data taking script fails because of the implemented hard limit of 1000 level crossings. About 1.5 days after the end of irradiation, scans were not failing anymore. Figure 7.16 shows the evolution of the fake-hit rate of this sensor over time. Immediately after the fake-hit rate falls below the hard cut limit, a fake-hit rate around the upper sensitivity limit is measured. Within the first 7 days, it drops by a factor of 10 to approximately $2 \cdot 10^1\,\mathrm{pixel}^{-1}\,\mathrm{s}^{-1}$. The next scan is taken only about one week later, where a fake-hit rate of $(3.93\ ^{+3.65}_{-0.31}) \cdot 10^1\,\mathrm{pixel}^{-1}\,\mathrm{s}^{-1}$ is found. In the following weeks, the fake-hit rate stays rather constant with a slight downwards trend. 67 days after the end of irradiation it is measured as $(2.78\ ^{+2.65}_{-0.26}) \cdot 10^1\,\mathrm{pixel}^{-1}\,\mathrm{s}^{-1}$, showing only a slight improvement over several weeks. In the last scan, only one pixel is found to be noisy. The GID-PID map can be seen in figure C.20. Only two clusters of (GID, PID) pairs are observed. Because every hits generates an assertion and a deassertion pulse in the output line, these two clusters show that in fact only one pixel on the pixel matrix is shows fake-hits. The other 1023 pixel seem to have fully recovered their low fake-hit rate by about two months of annealing at room temperature.

Anyway, it still has to be checked, whether all pixel respond to pulsing and external stimuli as for example X-rays. A threshold and a source scan are performed 96 days after the end of irradiation. All pixel respond to pulsing. In the source scan, the one noisy pixel (c=28, r=18) is masked. All other pixels show at least 3 hits in a scan of 50 000 trigger and are thus considered alive. The corresponding hitmaps are attached in figures C.21 and C.22. These results hint towards sufficient radiation hardness of the technology in terms of ionizing radiation for future experiments as the ALICE 3 Vertex Detector. However, only one sample has been irradiated to radiation doses high enough. For the sake of repeatability, a few more samples have to be irradiated to comparable doses in order to be able to make a final statement on the required radiation hardness. As also the irradiation in ALICE 3 will happen at a much lower dose rate than in the X-ray machine, it is furthermore of interest to study ongoing annealing processes in the already irradiated sample in the upcoming months. Lastly, the annealing happening in the ALICE 3 experiment might be lower than here, if it is finally decided to cool the chips to sub-zero temperatures in the experiment itself. The annealing of lower temperatures over longer durations also still has to be studied.

7.6 Annealing

After the end of irradiation, the chips are monitored as closely as possible with the amount of test systems and man power available. The chip temperature was controlled to 20 °C during measurements times and uncontrolled at room temperature ($\approx 20\,°\mathrm{C}$) otherwise. Figure 7.17 shows the evolution of the fake-hit rate of a sensor irradiated with 10 kGy. It is visible how the

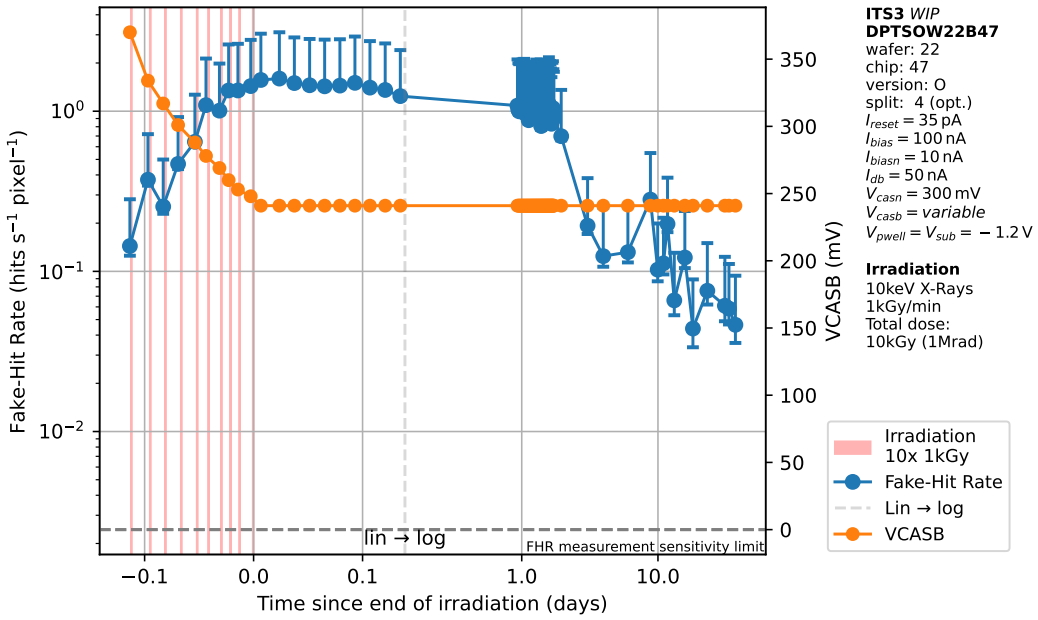


Figure 7.17: Fake-hit rate vs. time in a DPTS irradiated up to 10 kGy during and after irradiation. After end of irradiation, the chip was stored at $\approx +20\,^{\circ}C$.

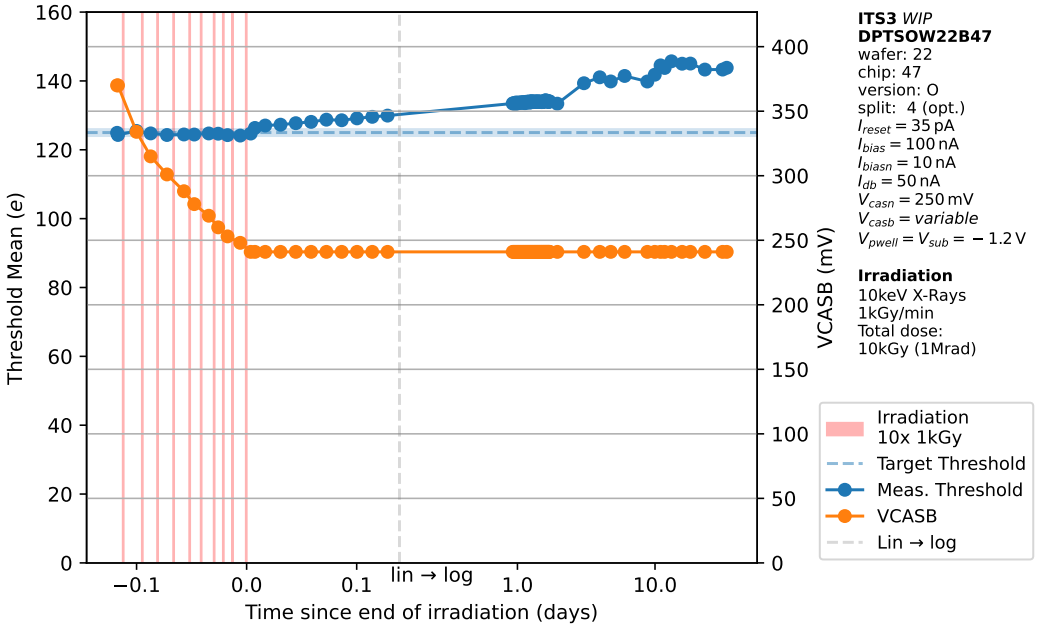


Figure 7.18: Threshold mean vs. time in a DPTS irradiated up to 10 kGy during and after irradiation. After end of irradiation, the chip was stored at $\approx +20\,^{\circ}C$.Caption

fake-hit rate drops down again after being at a rather high level at the end of the irradiation campaign. Within approximately 37 days, the fake-hit rate drops from $(1.60\ ^{+1.51}_{-0.07})$ pixel^{-1} s^{-1} to $(4.64\ ^{+4.76}_{-1.06}) \cdot 10^{-2}$ pixel^{-1} s^{-1}, effectively cutting it by almost two orders of magnitude. It is observed that the fake-hit rate after 37 days of annealing is even lower than it was initially before start of the first irradiation step. This could be explained by the fact that the mean threshold of the sensor is going up during annealing (see next paragraph) because no threshold tuning is performed in that period. By that time, the threshold has already increased to about 143 e. It has been observed in other chips that a threshold increase of about 20 e can cut the fake-hit rate in half and even more. It is thus not likely that the exposure to ionizing radiation and an extended period of annealing decreases the overall fake-hit rate of the sensor.

In figure 7.18, the before-mentioned threshold evolution during annealing is reported. Immediately after the end of irradiation, the measured mean threshold of the sensor begins to increase. This does, in the general trend, continue during the whole annealing period where data is available. As already mentioned, in the course of 37 days, the measured mean threshold has increased from 125 e to about 143 e, whereas there is some fluctuation of a few e between consecutive measurements. In general, the observed behavior already hints to annealing processes taking place in the sensors, as parts of the effects of the damage introduced by ionizing radiation are reducing over time. This means that the threshold lowered by ionizing radiation increases again during annealing and that the fake-hit rate decreases again after it increased due to the radiation damage. These results are also widely in line with the other chip that received an ionizing dose of 10 kGy. Plots for that chip are shown in figures C.14 and C.15. There, a sudden drop in fake-hit rate could be observed at one point. This can most likely be attributed to a power cycle of the chip, as this was also observed in other chips. The general results are also in line with what has been observed in annealing studies of the chips from the July 2022 irradiation campaign.

In figure 7.19, the fake-hit rate evolution of one of the 100 kGy chips is depicted. Here, the fake-hit rate recovers by more than two orders of magnitude during the course of 45 days. One day after the end of irradiation, the fake-hit rate suddenly drops from $(4.04\ ^{+3.90}_{-2.03}) \cdot 10^{1}$ pixel^{-1} s^{-1} to $(4.47\ ^{+4.31}_{-0.34}) \cdot 10^{-1}$ pixel^{-1} s^{-1}. Roughly 2 days pass by between both measurements. Here the chip was likely not mounted permanently in the test system thus effectively power cycling it. This is another hint towards high sensitivity of several chip observables to power cuts and re-powering. A systematic study of these effects was not yet done, but it is desirable. It could lead to increased understanding of the effects occurring during irradiation, if it could be pinned down, which of the several power domains (analog, digital, CML buffer) or which of the biasing voltages and currents (V_{casb}, V_{casn}, I_{reset}, I_{db}, I_{bias}, I_{biasn}) is responsible for this behavior.

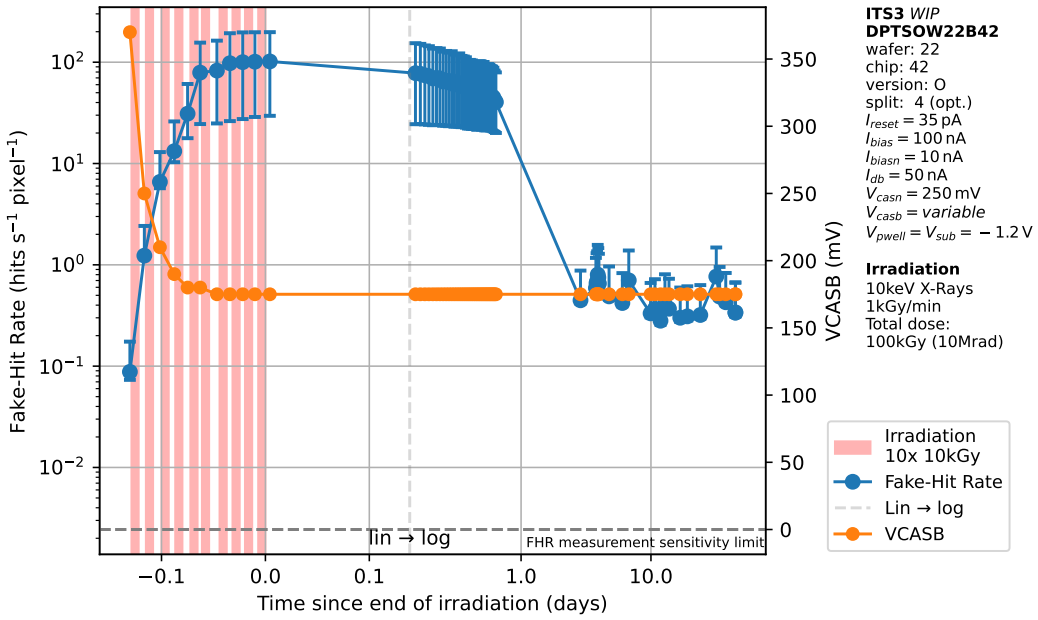


Figure 7.19: Fake-hit rate vs. time in a DPTS irradiated up to 100 kGy during and after irradiation. After end of irradiation, the chip was stored at ≈ +20 °C.

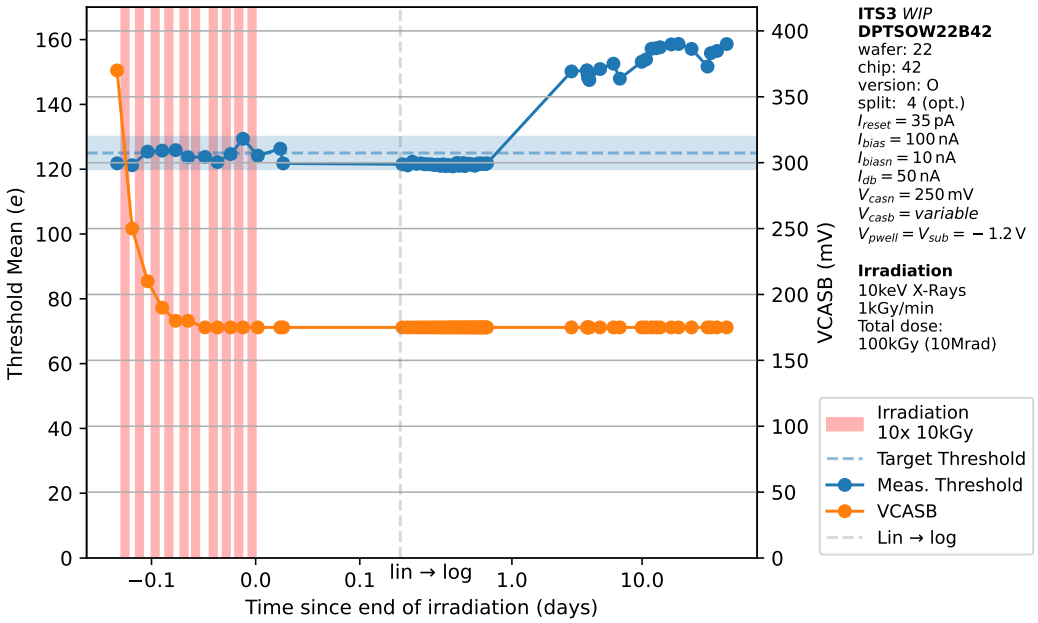


Figure 7.20: Threshold mean vs. time in a DPTS irradiated up to 100 kGy during and after irradiation. After end of irradiation, the chip was stored at ≈ +20 °C.

The evolution of the mean threshold is shown in figure 7.20. During the first day of annealing, no change of the threshold can be observed. In the following 45 days, the threshold increases from the tuned value of 125 e to about 159 e. The increase in threshold is higher than observed for the 10 kGy chip. On the one hand, the annealing duration is 8 days longer. On the other hand, if one reads the mean threshold after the 37 days of the 10 kGy chip, it becomes apparent that the difference in annealing duration can not be the only reason to explain this effect. During the irradiation of this sensor, V_{casb} has been lowered from 370 mV to 175 mV, which is a much higher difference than the 370 mV to 241 mV adjustment of the lower dose chip. This hints towards larger threshold drops introduced by a higher level of radiation dose. Therefore, there is also a larger margin of possible threshold recovery after the irradiation. The other chip at the same dose shows similar behavior as presented in figures C.16 and C.17. The only difference is that this chip shows a slight downward drift of the mean threshold by about 5 e within the first 2 days after the end of irradiation, before the well known increase in threshold sets in. It is yet unknown, why this shift can be observed. A possibly explanation could be that the temperature increased during measurement.

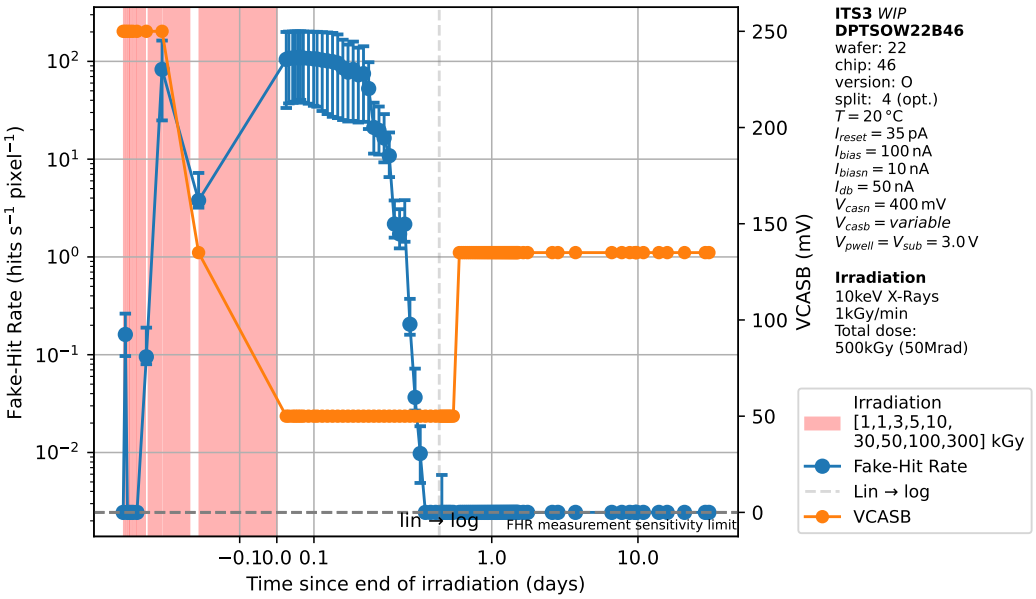


Figure 7.21: Fake-hit rate vs. time in a DPTS irradiated up to 500 kGy during and after irradiation. After end of irradiation, the chip was stored at ≈ +20 °C.

The fake-hit rate evolution for one of the 500 kGy sensors is shown in figure 7.21. Right after the end of irradiation, the fake-hit rate is about $1 \cdot 10^2\,\text{pixel}^{-1}\,\text{s}^{-1}$, being around the upper sensitivity limit. Already within the first day of annealing, the fake-hit rate drops down sharply towards the lower sensitivity limit. Even though the chip received 5 times more ionizing dose than the chip as previously discussed, the annealing effects appear to reduce the fake-hit rate much faster. This might be caused by the fact that the threshold mean

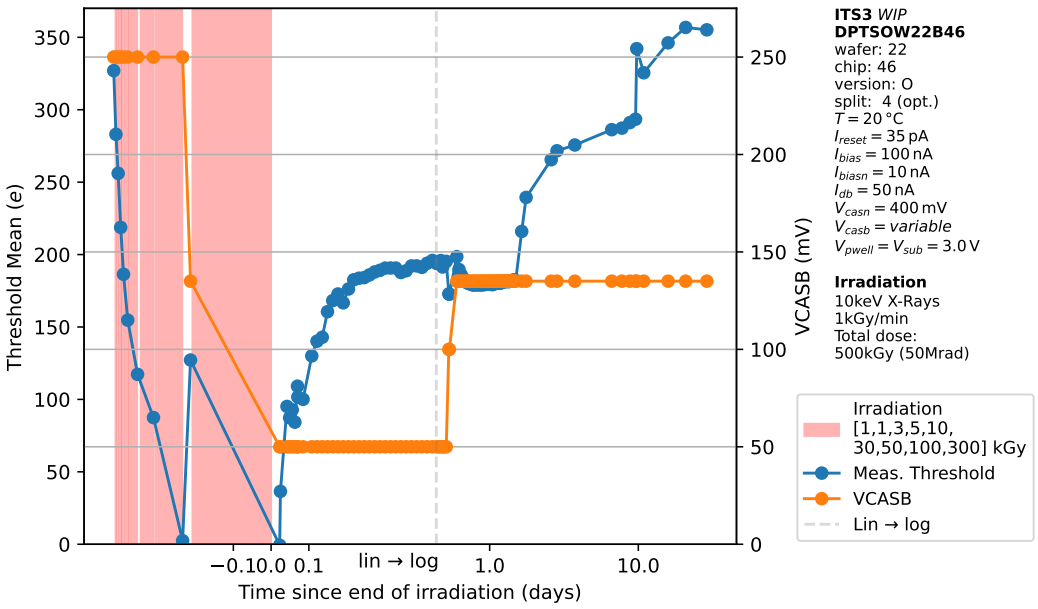


Figure 7.22: Threshold mean vs. time in a DPTS irradiated up to 500 kGy during and after irradiation. After end of irradiation, the chip was stored at $\approx +20\,^{\circ}\mathrm{C}$.

was initially tuned to 350 e, being in a naturally much less noisy regime. As the annealing continues, the dropped threshold also rises back up while bringing the chip to an operating point, which is effectively quiet.

The evolution of the threshold is shown in figure 7.22. Right after irradiation, the threshold finding algorithm fails, estimating the mean threshold to 0 e. In the minutes and hours after this, the mean threshold recovers quite quickly, after which a saturation around 190 e sets in. V_{casb} had to be lowered two times during the irradiation steps. It was decided to revert these changes as quickly as possible after the irradiation in order to keep a good comparability of results before and after irradiation. After about 1 day, V_{casb} is set back to 135 mV, which can operate the chip at a dose of 200 kGy. In the first period of time after this change, a drop of about only 10 e is visible. Before this period, the chip was moved from the X-ray machine to the laboratory, so potential temperature effects could play a role when trying to explain this behavior. After another day, the mean threshold starts increasing again, until 31 days after the end of irradiation, a mean threshold of 355 e is reached. This value is, in fact, close to the initially tuned threshold of 350 e. However, the chip is still operated at reduced V_{casb} with respect to the initially set 250 mV. Another increase of V_{casb} would be needed in order to compare the overall recovery of threshold within the first month of annealing. What can however be observed is that the mean threshold 31 days after irradiation is significantly higher than the 127 e observed after the first 200 kGy of irradiation, where V_{casb} was set to the same value.

It is therefore safe to say that the threshold-decreasing effect of the last 300 kGy is compensated for by 31 days of annealing. In fact, the measurements after 1 day already revealed higher mean thresholds than those observed immediately after the 200 kGy irradiation step. The other chip irradiated to 500 kGy shows the same general behavior, including the 10 e threshold drop after moving the chip to the laboratory. The reason for this can only be speculated, but it is not unlikely an effect of temperature increase under the light shielding cloth. This effect might also be related to the threshold drop of chip B43 presented in figure C.17 and discussed earlier in this section. Results from the other chip at 500 kGy are comparable and shown in figures C.18 and C.19.

7.7 Energy Calibration

For all chips of the March 2022 irradiation campaign, at least one ^{55}Fe source scan was taken before and at least one after the irradiation in order to study the effects of ionizing radiation on the energy calibration. Figure 7.23 shows the uncalibrated energy spectrum in terms of ToT (µs) before and after irradiation of DPTSOW22B44 with an ionizing dose of 500 kGy. The spectra are normalized to an area of 1. The spectra fit each other fairly well. The peak of the Mn-k$_\alpha$ is slightly smeared out towards higher ToT while decreasing also the height of the peak. The shift is in the order of 0.5 µs. Given the width of the peak, the shift is not very severe. In contrast to that, figure 7.24 shows the energy spectra with ToT correction applied. In other words, the calibration of ToT-vs.-V_h obtained from a non-linear calibration (cf. section 6.5) was applied in order to convert from ToT to pulsing voltage equivalents in units of mV. It catches the eye immediately that the spectrum after irradiation is shifted severely towards *lower* calibrated ToT with respect to the spectrum obtained before irradiation. This shift is approximately 200 mV large. The smearing which leads to a decrease of the normalized peak height is also observable here. As the uncorrected spectra show only a very minor shift, which is why it is reasonable to assume that the charge collection properties of the sensor themselves are largely unaffected by ionizing radiation. A larger shift only becomes apparent when applying the ToT-vs.-V_h calibration. Thus, the assumption is that it is in fact this calibration, which is affected by ionizing radiation. It could be explained by the fact that this calibration is obtained by repeatedly pulsing the pixel with different pulsing voltages V_h. The functional diagram of the DPTS (cf. figure 5.4) indicates that there is pulsing circuitry present in the pixel matrix. As ionizing radiation is known to have effects on transistor circuits (cf. section 3.3.1), it is straightforward to assume that the ionizing radiation led to damages in the pulsing circuitry, thus injecting too large or too little charge into the pixel, which leads to shifting curves of the ToT-vs.-V_h and consequently to

incorrectly calibrated ToT. Although everything is hinting into this direction, this hypothesis will need a more systematic verification.

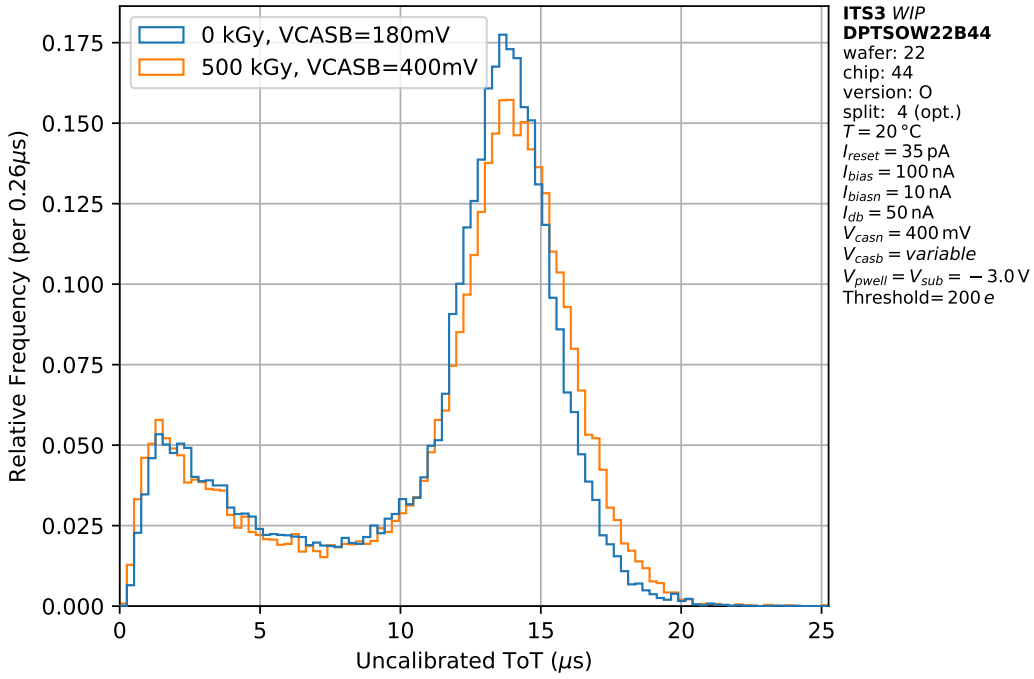


Figure 7.23: Uncorrected ToT spectra from a ^{55}Fe source scan before and after irradiation of a single chip. The threshold was tuned to 200 e individually before and after. The spectra are normalized to an area of 1 µs.

Consequently, after applying the Mn-K_α fits, one finds that the injected charge calibration factor η apparently shifts from 1.054 ± 0.001 to 1.117 ± 0.001 by irradiating the sensor with 500 kGy X-rays. It is debatable how this has to be interpreted and further studies on this will be needed. This will also affect the decision, whether the appropriate way of dealing with this is either taking one η at every radiation dose or if the η taken at zero radiation dose is in fact the value to be used for all later doses, as the damage only affects pulsing and not the charge collection itself.

The ^{55}Fe spectra for the other chips from the March 2022 campaign (with exception of B22 with 5 MGy) are comparable. An apparent shift of the injected charge calibration factor is observed in all of them. Table 7.3 reports the measured injected charge calibration factors before and after irradiation. It is also easily visible that $\Delta\eta = \eta_{\text{after}} - \eta_{\text{before}}$ increases with increasing ionizing dose. This underlines the hypothesis that the shift of calibrations is actually caused by the ionizing radiation and not by other effects.

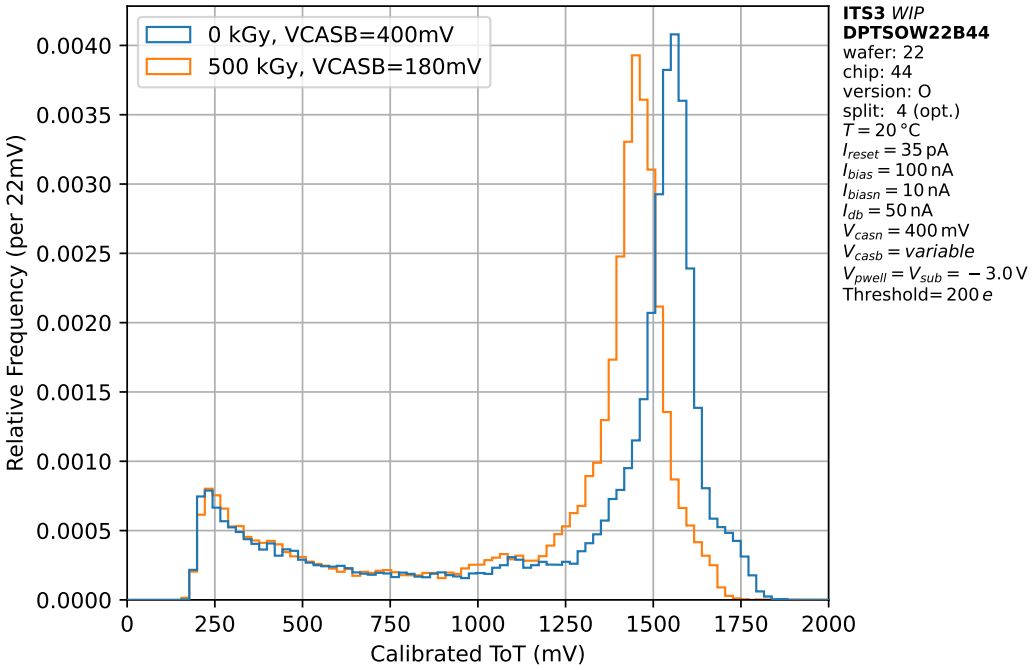


Figure 7.24: Corrected ToT spectra from a ^{55}Fe source scan before and after irradiation of a single chip. The threshold was tuned to 200 e individually before and after. The spectra are normalized to an area of 1 mV.

Table 7.3: Injected charge calibration factors η of six DPTS with different levels of ionizing radiation before and after their irradiation. The chips were stored at $\approx +20\,°C$ after irradiation.

ID	Dose	Annealing Duration	η_{before}	η_{after}	$\Delta\eta$
DPTSOW22B45	10 kGy	81 d	1.045 ± 0.003	1.080 ± 0.001	0.035 ± 0.004
DPTSOW22B47	10 kGy	81 d	1.085 ± 0.002	1.114 ± 0.001	0.029 ± 0.004
DPTSOW22B42	100 kGy	81 d	1.044 ± 0.004	1.104 ± 0.001	0.060 ± 0.005
DPTSOW22B43	100 kGy	83 d	1.100 ± 0.002	1.150 ± 0.008	0.050 ± 0.009
DPTSOW22B44	500 kGy	80 d	1.054 ± 0.001	1.117 ± 0.001	0.063 ± 0.002
DPTSOW22B46	500 kGy	81 d	1.056 ± 0.001	1.107 ± 0.001	0.061 ± 0.002

7.8 Efficiency

A subset of sensors mentioned in this chapter has been tested in test beams to determine the sensor efficiency after exposure to ionizing radiation. All available data sets are listed in table 7.4. A back bias of $V_{\mathrm{bb}} = -2.4\,\mathrm{V}$ is chosen in order to keep all chips operational, while not unnecessarily increasing the back bias too much into the negative direction. At this back bias, the standard tuned V_{casn} value of 350 mV is applied. Furthermore, the default settings for irradiated chips of $I_{\mathrm{reset}} = 35\,\mathrm{pA}$ and $I_{\mathrm{db}} = 50\,\mathrm{nA}$ are used. V_{casb} is used to control the threshold as usual. A scan over different thresholds, and therefore also different V_{casb} values, is taken for every chip. The other parameters are used as listed in table 6.1. For the ALPIDE chip of the ITS2, detection efficiencies of $> 99\,\%$ where measured [Agl+23]. Given that the detection efficiency should not be lower after the ITS3 upgrade, 99 % are targeted as a first efficiency benchmark here.

Table 7.4: Overview on beam test data sets from sensors which have been exposed to ionizing radiation. *Note that 500 kGy where already present for 305 d. For detailed irradiation logs see section 7.1 and tables 7.1 and 7.2.

ID	Dose	Annealing Duration	Ann. Temp.	Test Beam Site	Particles
DPTSOW22B26	10 kGy	2 d	−20 °C	CERN PS	10 GeV/c pos. hadrons
DPTSXW22B8	100 kGy	3 d	−20 °C	CERN PS	10 GeV/c pos. hadrons
DPTSSW22B22	500 kGy	5 d	−20 °C	CERN PS	10 GeV/c pos. hadrons
DPTSSW22B22	500 kGy	158 d	−20 °C	DESY II	3.4 GeV/c electrons
DPTSSW22B22	5000 kGy	58 d*	+20 °C*	CERN PS	10 GeV/c pos. hadrons

It is worth noting again that the expected and thus required ionizing radiation hardness for the ITS3 is 10 kGy [Mus19]. The lowest of the tested doses is therefore already enough to allow a statement about the viability of using the *TPSCo.* 65 nm CMOS technology for the ITS3 project. Higher doses are still tested to scope the operational margin of this technology in view of the ALICE 3 project, where ionizing doses in the order of 3000 kGy (cf. chapter 7) will be expected. Figure 7.25 shows the measured efficiencies in a single graph. In the dataset of the chip with 5000 kGy, four very noisy pixel ($< 0.4\,\%$ of the whole matrix) have been masked in analysis.

The non-irradiated reference sensor is, at chosen parameters, not noisy over the whole tested threshold range. It is able to reach $> 99\,\%$ efficiency up to a mean threshold of about 160 e Furthermore, it can be observed that the sensor irradiated up to 10 kGy reaches an efficiency of $> 99\,\%$ over a wide range of threshold, especially where the fake-hit rate of the sensor is still at the measurement sensitivity limit. Only at about 180 e mean threshold, the efficiency begins to drop below 99 %. This behavior is even better than in the non-irradiated reference chip. Anyhow, this is more likely to be caused by chip-to-chip variation, as ionizing radiation

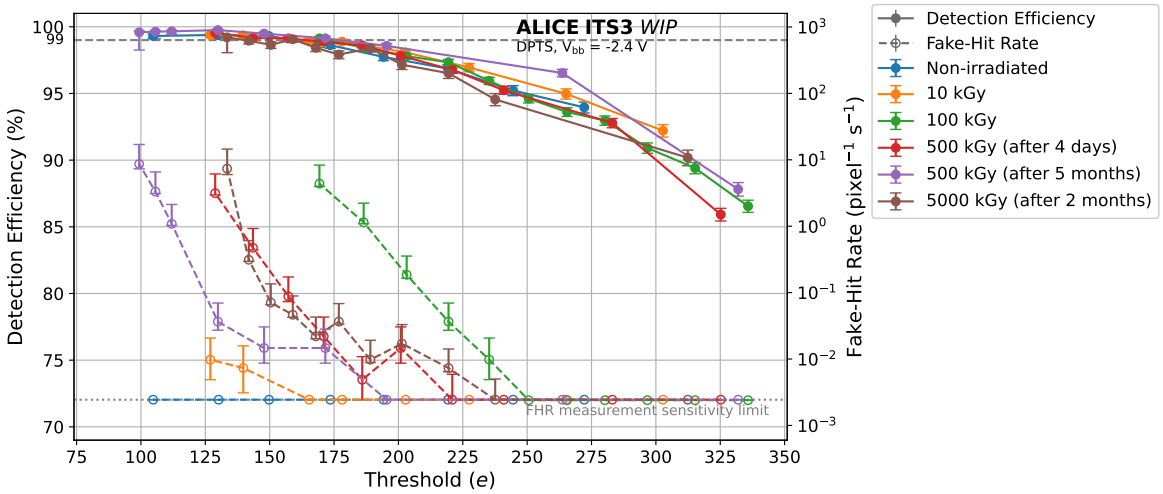


Figure 7.25: Efficiency and fake-hit rate vs. threshold for sensors with different levels of ionizing radiation. Details about annealing periods can be found in table 7.4.

is not expected to increase the performance of the sensor. The radiation hardness for ionizing radiation can thus be considered verified for doses expected in the ITS3.

The sensor irradiated to 100 kGy shows the same general trend of efficiencies dropping below 99 % around 180 e mean threshold. However, this sensor shows fake-hit rates significantly higher than all the other chips tested. At a threshold of 186 e, the fake-hit rate is already at a value of $(1.14\ ^{+1.08}_{-0.05})$ pixel^{-1} s^{-1}, whereas at the same threshold the 10 kGy chip is still at the measurement sensitivity limit. As seen in table 7.4, 3 days have passed between the end of the irradiation and of the test in the test beam. It is observed that the fake-hit rate lowers rather quickly after the end of irradiation. However, the chip irradiated to 500 kGy was tested with only one day more annealing time after irradiation. Despite having received 5 times the radiation dose, the onset of noise is shifted by about 30 e towards lower thresholds and at equal thresholds the chip with the higher dose is at least one order of magnitude less noisy than the 100 kGy chip. For these reasons, this chip is considered to be more noisy on the base of chip-to-chip variation rather than due to the radiation. To verify this, at least one or two more DPTS should be tested at equal parameters (dose, biasing, annealing duration). Nevertheless, such sensors with varying operational behavior have to be studied in view of the ITS3 as even with probing chips already on the wafer, in contrast to the ITS2, only full wafer can be selected for usage in the final detector. Therefore, it is important to know how large the spread of operational performance is.

The data from the chip at 500 kGy is particularly interesting because this chip was measured twice, once 4 days after irradiation and another time 5 months after irradiation. Efficiencies vs. mean thresholds are again generally comparable, also with the results from the chips with

lower doses. In fact, it is observed that the efficiency is slightly higher over all thresholds after 5 months of annealing (at $-20\,^{\circ}\mathrm{C}$). However, 99 % efficiency are still reached in both cases up to about $170\,e$. On the other hand, the annealing also lets the fake-hit rate decrease. The onset of noise is shifted by about $50\,e$ towards lower threshold just by waiting about 5 months. This fact is in line with the observed fake-hit rate vs. time behavior studies in previous sections.

Lastly, the same sensor is irradiated with another 4500 kGy. After an annealing period of 2 months, the sensor is tested again in a beam test. For more details on this see sections 7.1 and 7.5. The fake-hit rate behavior is comparable to the same sensor after 500 kGy and 4 days of annealing. The efficiencies are found to be marginally lower than measured at 500 kGy for this same chip. However, 99 % efficiency are still reached at some of the threshold points. The measurements shows that the efficiency is on the edge of what is acceptable for future detectors.

This result can be considered a first step towards the validation of the *TPSCo.* 65 nm CMOS technology for ionizing radiation levels as expected in ALICE 3. However, a more detailed study is needed, whereas at least one more chip has to be irradiated and tested at the same dose level. Moreover, as the ALICE 3 experiment will be running several years, time is a significant factor and the annealing behavior has to be studied in more detail. Finally, the temperature dependency has to be taken into account, as possibly, the MAPS used for the ALICE 3 Vertex Detector could be cooled down to $-25\,^{\circ}\mathrm{C}$ to cope with the high level of non-ionizing radiation during the operation. If the temperature will actually be lowered, annealing has also to be taken into account again, since a lower temperature is expected to suppress annealing processes.

7.9 Summary

It can be concluded that the effects of ionizing radiation influence the sensor operation of the DPTS. The main results are:

- The fake-hit rate rises with increasing ionizing radiation load, but annealing lets the fake-hit rate drop down again fairly fast.
- The threshold is lowered by ionization damage. Annealing effects let the threshold rise back up, but not as fast as the fake-hit rate recovers.
- The threshold shift can be compensated for by changing the biasing parameters. This works over a wide range of doses, at least up to 200 kGy.

- The ToT-vs.-V_{h} calibration is shifting, leading to a seemingly changing deviation in the energy calibration. This is likely an effect of ionizing radiation shifting operating points of the pulsing circuitry.
- At the expected ionizing radiation dose of the ITS3, $> 99\,\%$ efficiency at low fake-hit rate are easily reachable
- Even at 5 MGy ionizing dose and operation at $+20\,^{\circ}\mathrm{C}$, efficiencies of close to 99 % with tolerable fake-hit rate can be achieved at a tolerable fake-hit rate and approximately 2 months of annealing at $20\,^{\circ}\mathrm{C}$.

These results are an important step towards the validation of ionizing radiation hardness of the *TPSCo.* 65 nm CMOS technology, indicating sufficient radiation hardness to be in the range of what is feasible. However, further studies have to be carried out.

8 Non-Ionizing Radiation

This chapter focuses on the effects of non-ionizing radiation on the DPTS sensors. Primarily, it will be studied, how different non-ionizing doses change the temperature dependency of the chip operation. Looking forward to the ITS3 upgrade, a non-ionizing dose of $10^{13}\,1\,\mathrm{MeV}\ \mathrm{n}_{eq}\ \mathrm{cm}^{-2}$ is expected over the duration of run 4 [Agl+23]. The ALICE 3 Vertex Detector will be installed in a much more harsh radiation environment. Over the duration of runs 5 and 6, the expected non-ionizing dose will be in the order of [Col22a, Table 1]

$$50\,\mathrm{months} \cdot 1.8 \cdot 10^{14}\,1\,\mathrm{MeV}\ \mathrm{n}_{eq}\ \mathrm{cm}^{-2}/\mathrm{month} \approx 9 \cdot 10^{15}\,1\,\mathrm{MeV}\ \mathrm{n}_{eq}\ \mathrm{cm}^{-2}, \tag{8.1}$$

not yet including a safety factor.

8.1 Setup

The effects of non-ionizing radiation are tested by irradiating the sensors with neutrons from a nuclear reactor at JSI Ljubljana, Slovenia. Neutrons are used as they introduce only little ionization damage, which helps disentangling both damage mechanisms. $1\,\mathrm{MeV}\ \mathrm{n}_{eq}\ \mathrm{cm}^{-2}$ introduces additional $2{\cdot}10^{-18}\,\mathrm{kGy}$ in silicon via recoils. At the highest dose of $10^{16}\,1\,\mathrm{MeV}\ \mathrm{n}_{eq}\ \mathrm{cm}^{-2}$, the additional 0.02 kGy should be negligible if compared to results from chapter 7. [Spi05] There were DPTS chips irradiated to doses of 10^{13}, 10^{14}, 10^{15}, $2 \cdot 10^{15}$, $5 \cdot 10^{15}$ and $10^{16}\,1\,\mathrm{MeV}\ \mathrm{n}_{eq}\ \mathrm{cm}^{-2}$ and available to be tested. Tests of the chips before and during irradiation can not be performed, because the space within the reactor access tube is very limited. Therefore, the diced chips are irradiated standalone and only mounted to the carrier after the end of the irradiation. From the arrival at CERN on, the chips are stored at $-20\,^{\circ}\mathrm{C}$ to slow down annealing. This ensures that observed radiation damages can be associated with the known neutron doses. Before measurement, the chips have to be brought to room temperature and dried completely to avoid electrical damage. The measurement time should be as short as possible to minimize annealing.

To protect the chip from condensation, the temperature must be kept be some °C above the dew point, which at lab conditions lies usually around $10\,^{\circ}\mathrm{C}$. The lower endpoint of

the measurement range is thus set to 15 °C. As mentioned in chapter 6, one type of water cooler is also able to heat the cooling water and consequently the chip up to 40 °C, which is used as the upper endpoint of the measurement range. The available range is sampled in steps of 5 °C by a custom scanning script. The temperature is set on the chiller via remote connection. To ensure full thermalization of the chip, a delay of 15 min is awaited after the water temperature reaches its nominal target temperature. At all temperatures, a threshold scan, a fake-hit rate scan and a decoding calibration are taken. For the measurement program with ^{55}Fe source, additional ToA and source scans are taken at every temperature. Following the same reasoning as in chapter 7, no injected charge calibration factors are applied here, with exception of the section on the efficiency 8.4.

8.2 Temperature Dependency

In this section, the effects of the sensor temperature on various observables are discussed. Since these behaviors are expected to change with non-ionizing radiation dose, all measurements are carried out on a non-irradiated chip, a 10^{13} 1 MeV n_{eq} cm^{-2}, a 10^{14} 1 MeV n_{eq} cm^{-2}, and a 10^{15} 1 MeV n_{eq} cm^{-2} chip. Higher radiation levels are not easily operable at room temperature and will be discussed separately in the last section of this chapter. As for ionizing radiation, two approaches are taken here: keeping all the chip biases constant over change of radiation dose and tuning V_{casb} in order to keep the threshold at a constant level. With the first approach, what impact a temperature change has if also the radiation dose is changed can be studied. The second approach can then be used to disentangle whether a change in certain observables is a consequence of the irradiation or if it is because the threshold has shifted. Since ^{55}Fe source scans are very much dependent on the applied threshold, these scans are only carried out with the tuned-threshold approach.

In previous measurements, it became apparent that neutron-irradiated chips require increased I_{reset} for proper operation. This is, because the leakage current is rising (cf. sections 3.1 and 3.3.2) and it has to be compensated for by an increased reset current. It was found that increasing I_{reset} to 35 pA and decreasing I_{db} to 50 nA works sufficiently. For comparability, these parameters are used for all chips. Furthermore, $V_{\text{bb}} = -1.2$ V and $V_{\text{casn}} = 250$ mV are used.

8.2.1 Constant Biasing Parameters

Starting from the nominal chip biases (cf. table 6.1), V_{casb} is reduced to 200 mV to move the chips to a less noisy regime. In figure 8.1, the temperature curves of the fake-hit rate of the four different irradiation doses can be seen. The non-irradiated and the 10^{13} 1 MeV n_{eq} cm^{-2}

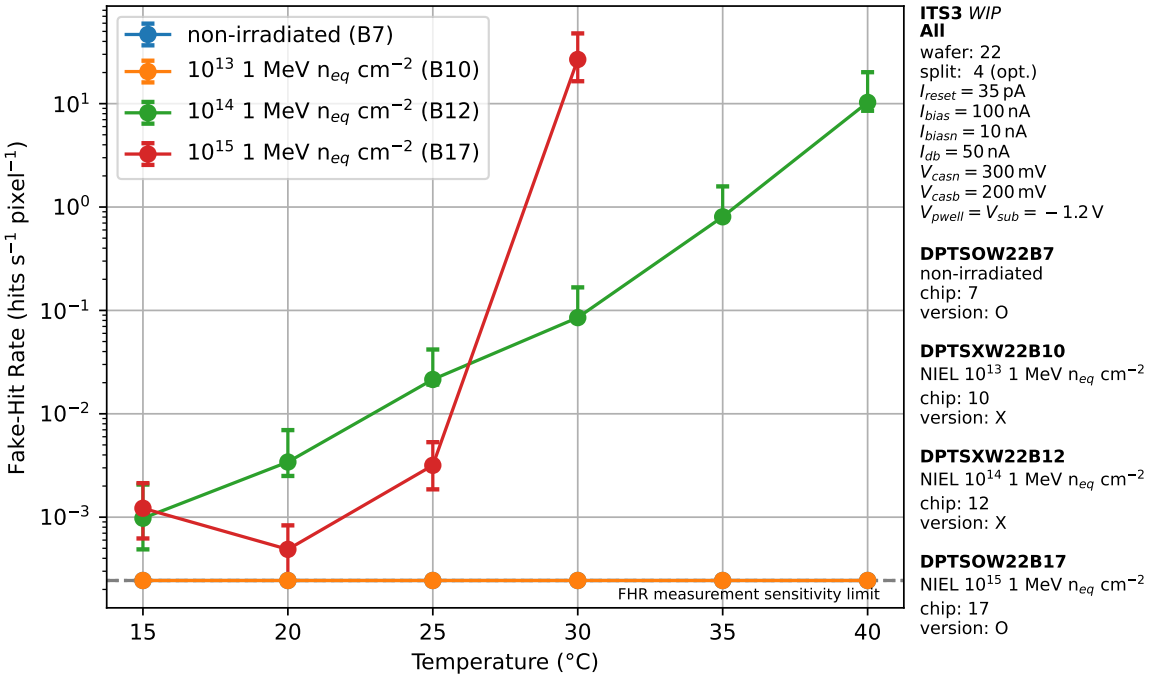


Figure 8.1: Fake-hit rate vs. temperature for different levels of non-ionizing radiation dose at constant biasing. The data points for the non-irradiated and for the 10^{13} 1 MeV n_{eq} cm^{-2} chip overlap at the sensitivity limit.

chip are not noisy and show a fake-hit rate at the sensitivity limit over the whole temperature range. For 10^{14} 1 MeV n_{eq} cm^{-2} the fake-hit rate is about 10^{-3} $pixel^{-1}$ s^{-1} at 15 °C and monotonously increasing with increasing temperature up to about 10^{1} $pixel^{-1}$ s^{-1} at 40 °C. Considering the logarithmic y-axis, the increase in fake-hit rate is assumed to be exponential with increasing temperature as the slope is almost constant. At 20 °C the 10^{15} 1 MeV n_{eq} cm^{-2} chip lies one order of magnitude below the 10^{14} 1 MeV n_{eq} cm^{-2} chip. This is likely an effect of chip-to-chip variation as even in non-irradiated samples, the fake-hit rate is observed to differ substantially (cf. chapter 7). Going to lower or higher temperatures, the fake-hit rate increases. The trend towards lower temperatures opposes the general trend of increasing temperature leading to increased fake-hit rate.

One possible explanation for this is that the threshold of the sensor is also very temperature dependent (see later in this chapter) and a shifting threshold can also change the fake-hit rate. This can potentially be verified later in the measurement with constant threshold in section 8.2.2. On the other hand, the uncertainty intervals are overlapping partially, so that this also could be a statistical fluctuation. Towards higher temperatures, the increase in fake-hit rate is steeper than for the 10^{14} 1 MeV n_{eq} cm^{-2} sensor. To sum up, it is observed that the fake-hit rate is temperature dependent and this temperature dependency is increasing with increasing level of non-ionizing dose.

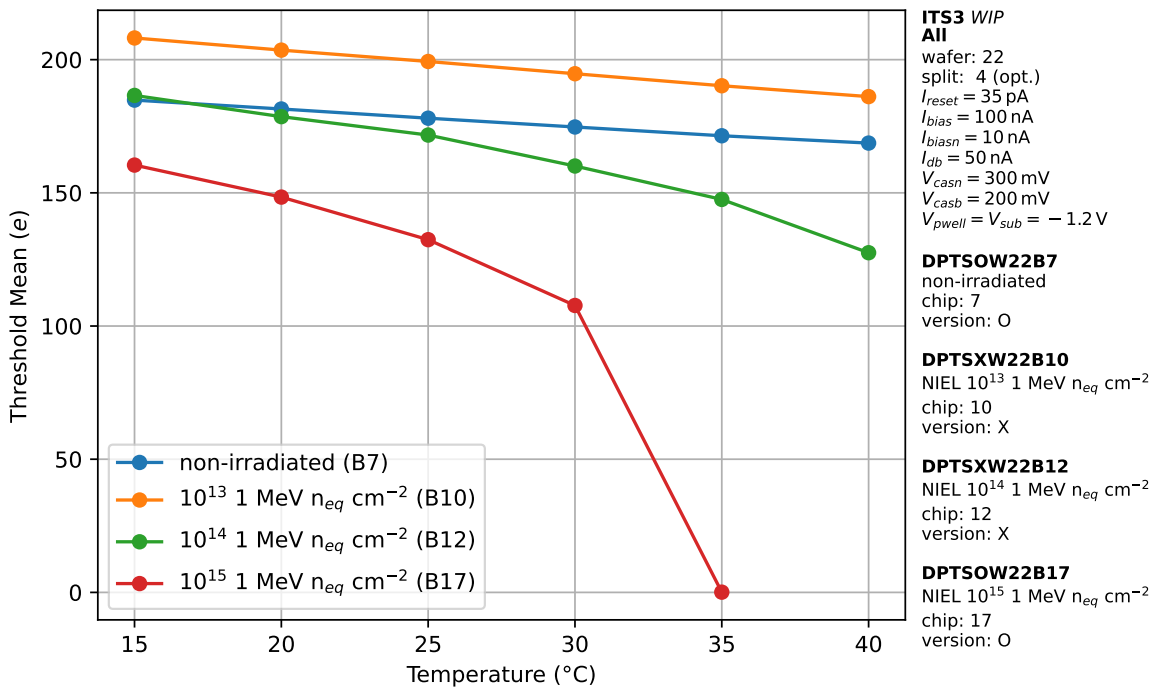


Figure 8.2: Mean threshold vs. temperature for different levels of non-ionizing radiation dose at constant biasing. For the $10^{15}\,1\,\mathrm{MeV}\ \mathrm{n}_{eq}\ \mathrm{cm}^{-2}$ chip at 35 °C, the threshold finding algorithm is failing giving a mean threshold of $0\,e$. This can be interpreted as unusable operating point.

Figure 8.2 shows the temperature curves for the threshold mean of the four tested chips. At 15 °C, there is already a threshold spread of about $50\,e$ between different sensors. This may be explained by chip-to-chip variation. For increasing temperature the trend is decreasing threshold at all dose levels including no irradiation. For the non-irradiated sensor, the decrease in threshold is rather constant with a slope of about $-0.6\,e\,\mathrm{K}^{-1}$. This increases to about $-0.9\,e\,\mathrm{K}^{-1}$ at a dose of $10^{13}\,1\,\mathrm{MeV}\ \mathrm{n}_{eq}\ \mathrm{cm}^{-2}$. At $10^{14}\,1\,\mathrm{MeV}\ \mathrm{n}_{eq}\ \mathrm{cm}^{-2}$ the slope is not constant anymore, but decreasing with decreasing temperature. Similar is observed for the $10^{15}\,1\,\mathrm{MeV}\ \mathrm{n}_{eq}\ \mathrm{cm}^{-2}$ chip up to 30 °C. The slope is again decreasing, but at a faster rate than at lower doses. Above this temperature, the chip stops working for this specific set of parameters. As the conductivity of silicon is strongly temperature-dependent, it could expected that the operating point of the front-end circuit changes with changing temperature. In this particular circuit, this manifests as decreasing mean threshold. With increasing non-ionizing irradiation level, the leakage current of the sensor is expected to rise. Also this can influence the operation of the front-end, which in this case leads to an increased temperature dependency of the mean threshold.

Another important aspect is the temperature dependency of the decoding calibration. It has been found previously that the decoding calibration depends on the applied back bias

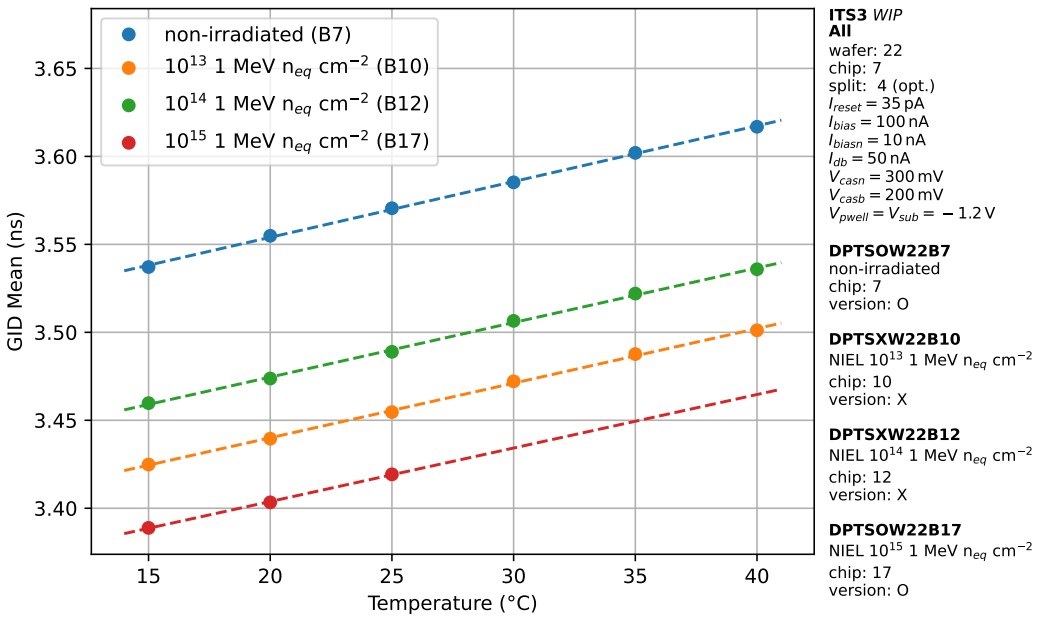


Figure 8.3: GID mean vs. temperature at constant biasing parameters for different levels of non-ionizing irradiation. The data is fitted with a linear fit of the form $a \cdot T + b$. The fit parameters are listed in table 8.1.

V_{bb} but not on other biasing parameters. Here it will be studied whether non-ionizing radiation damage and temperature can influence the decoding calibrations. Figure 8.4 shows the mean PID of all CoGs in a decoding calibration (cf. section 6.6) for different neutron doses over a temperature range. The fits are linear of the form $a \cdot T + b$, where a is the temperature coefficient, T the temperature and b an offset. It is immediately observable that the temperature has an impact on the GID and PID. Increasing temperature corresponds to longer GID and PID times. However, the neutron level does not influence the decoding calibration, as there is no particular order of the curves visible. The difference in y-intercept can be explained by chip-to-chip variation, which also occurs in non-irradiated samples (cf. figure C.23). The opposite behavior is observed for the PID, where the non-irradiated chip shows the lowest temperature coefficient with $(6.826 \pm 0.015)\,\mathrm{ps\,K^{-1}}$ and increasing coefficients towards $(7.371 \pm 0.040)\,\mathrm{ps\,K^{-1}}$ for the $10^{15}\,1\,\mathrm{MeV\ n_{eq}\ cm^{-2}}$ sample. This study again shows the importance of in-situ calibration measurements in every setup, as there is a strong temperature dependence of PID and GID at any NIEL-dose.

8.2.2 Tuning for Constant Threshold

In this section, the threshold is tuned to $125\,e$ for every chip and temperature separately by adjusting V_{casb}. The resulting V_{casb} values can be found in table 8.2. As already observed in the previous chapter, it is not possible to find an operating point at $10^{15}\,1\,\mathrm{MeV\ n_{eq}\ cm^{-2}}$

Table 8.1: Fit parameter of the temperature curves presented in figure 8.3 and figure 8.4.

Type	Chip ID	Dose in $1\,\mathrm{MeV\ n_{eq}\ cm^{-2}}$	Temperature Coefficient a in $\mathrm{ps\,K^{-1}}$	Offset b in ns
GID	B7	None	3.170 ± 0.041	3.491 ± 0.002
	B10	10^{13}	3.104 ± 0.050	3.378 ± 0.002
	B12	10^{14}	3.103 ± 0.052	3.412 ± 0.002
	B17	10^{15}	3.041 ± 0.082	3.343 ± 0.003
PID	B7	None	6.826 ± 0.015	7.807 ± 0.001
	B10	10^{13}	7.172 ± 0.113	7.500 ± 0.004
	B12	10^{14}	7.152 ± 0.110	7.579 ± 0.004
	B17	10^{15}	7.371 ± 0.040	7.374 ± 0.002

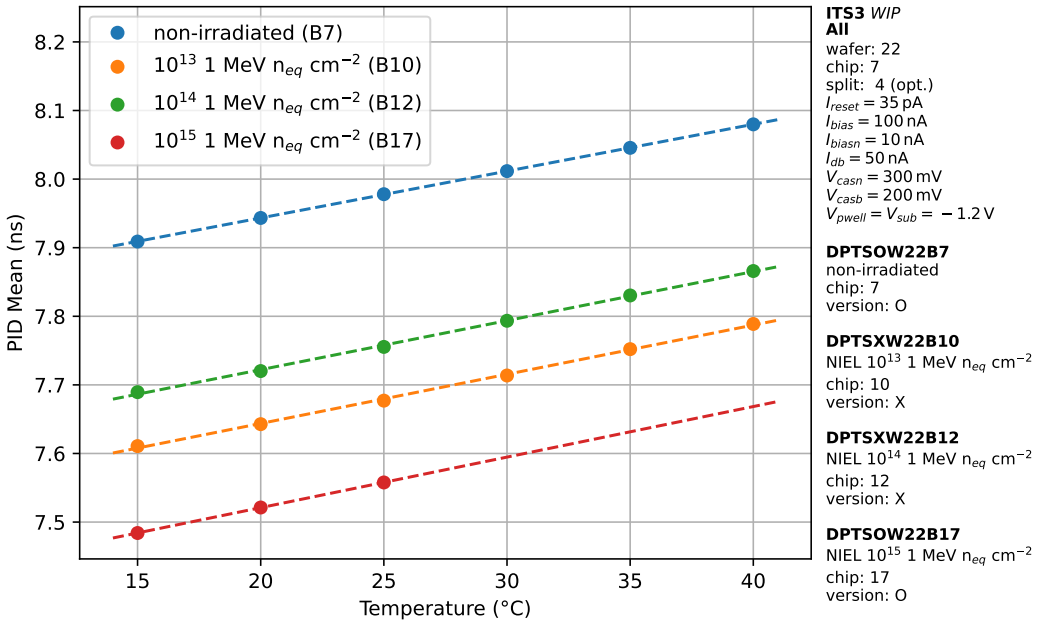


Figure 8.4: PID mean vs. temperature at constant biasing parameters for different levels of non-ionizing irradiation. The data of the mean PID is fitted with a linear fit of the form $a \cdot T + b$. The fit parameters are listed in table 8.1.

Table 8.2: Tuned V_{casb} values for neutron-irradiated chips to reach a threshold of $125\,e$. Chip B17 is not able to reach $125\,e$ above $30\,^{\circ}\mathrm{C}$. The tuning was performed only on a subset of four rows of the matrix.

Chip ID	Dose in $1\,\mathrm{MeV\ n_{eq}\ cm^{-2}}$	V_{casb} at $15\,^{\circ}\mathrm{C}$	$20\,^{\circ}\mathrm{C}$	$25\,^{\circ}\mathrm{C}$	$30\,^{\circ}\mathrm{C}$	$35\,^{\circ}\mathrm{C}$	$40\,^{\circ}\mathrm{C}$
B7	None	382 mV	372 mV	362 mV	353 mV	344 mV	336 mV
B10	10^{13}	372 mV	362 mV	353 mV	343 mV	335 mV	326 mV
B12	10^{14}	334 mV	321 mV	305 mV	285 mV	262 mV	226 mV
B17	10^{15}	287 mV	267 mV	237 mV	170 mV	-	-

and 35 °C or above when only varying V_{casb}. For this chip, all measurements are thus carried out only up to 30 °C.

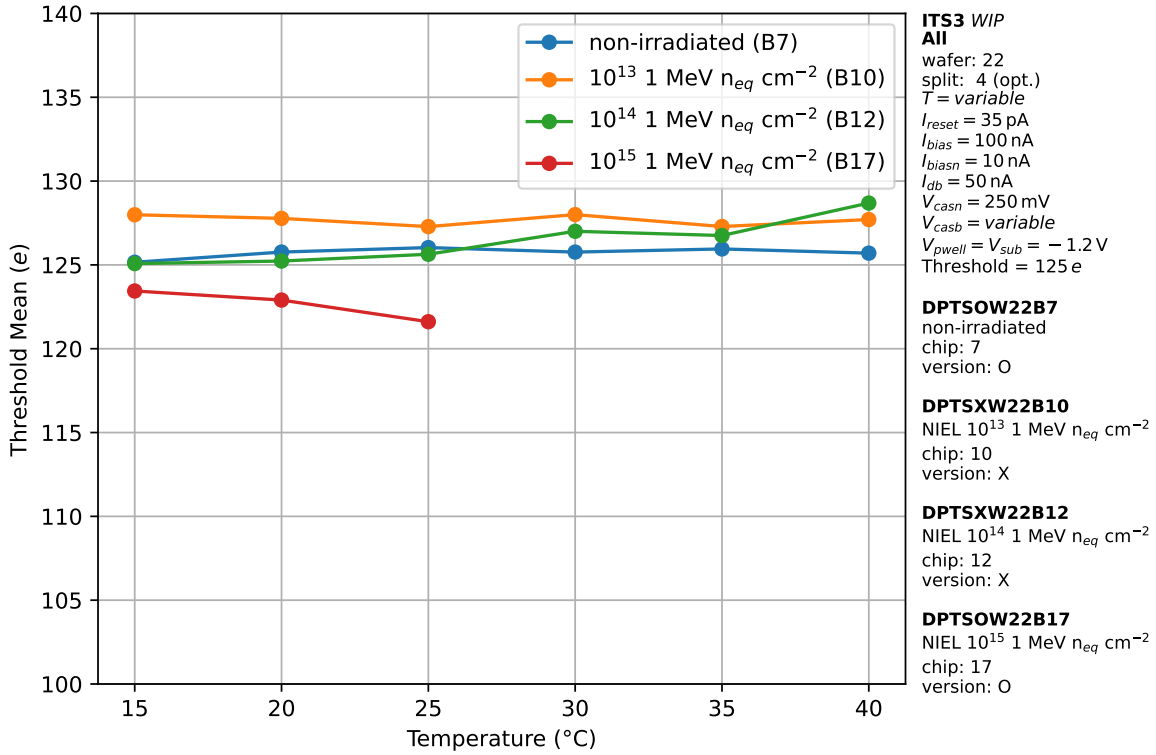


Figure 8.5: Temperature evolution of the mean threshold with already tuned V_{casb} values applied. This scan was performed on the whole matrix.

To verify the threshold tuning, figure 8.5 shows the temperature curve for the mean threshold. Although the curves do not fully overlap, all measured threshold fall in a range of about 5 e. A small deviation could be explained by the fact that the threshold tuning was performed on a subset of only four rows of the matrix to speed up the process. The final scan with tuned V_{casb} is however done on the whole matrix, so that there could be a systematic shift by the selection of certain pixel. For the purpose of these measurements, 5 e of mean threshold difference will likely not have much impact. Moreover, the threshold mean can also be shifted by the presence of noisy pixel in a row, following the arguments delivered in appendix B. The threshold scan at 10^{15} 1 MeV n_{eq} cm^{-2} and 30 °C over the whole matrix shows so many noisy pixel that the calculation of the threshold delivered an unrealistically high negative value of about $-5 \cdot 10^{18}$ e. This is most likely an artifact of the numerical differentiation used in the threshold calculation algorithm. This scan is excluded in further analyses.

In figure 8.6, the temperature-dependent fake-hit rates with tuned thresholds are reported. Also at this (lower) threshold, the non-irradiated and the 10^{13} 1 MeV n_{eq} cm^{-2} chips are so quiet that the measurement is at its sensitivity limit. However, in contrast to the constant

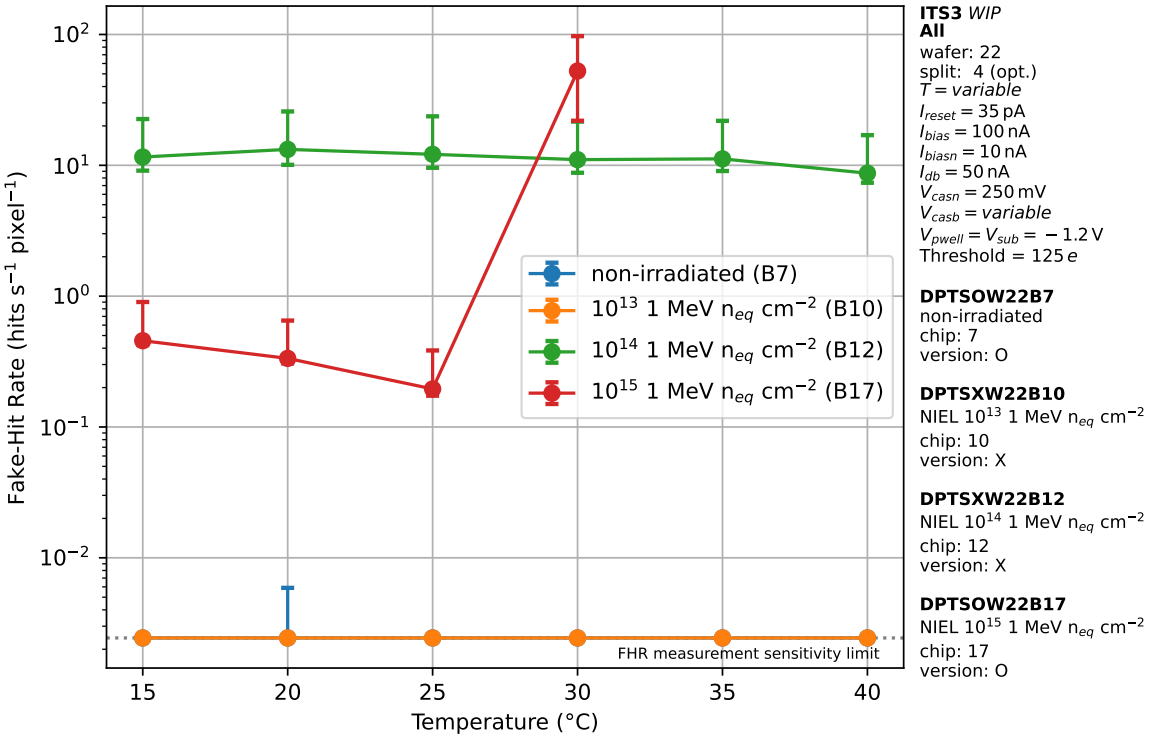


Figure 8.6: Fake-hit rate in dependency of temperature and neutron-dose with threshold tuned to 125 e.

V_{casb} measurement, the fake-hit rate of the 10^{14} 1 MeV n_{eq} cm^{-2} sensor is not dependent on the temperature anymore, since all data points fall into one uncertainty interval of each other. This indicates that the fake-hit rate on the sensor is intrinsically not temperature dependent. To this date, no detailed studies of the nature of noise in the DPTS chips has been carried out, but this results indicates that thermal noise play no dominant role here. The curve of the 10^{15} 1 MeV n_{eq} cm^{-2} shows a slight downward trend up to 25 °C starting from a generally lower fake-hit rate level than the 10^{14} 1 MeV n_{eq} cm^{-2} chip of about $5 \cdot 10^{-1}$ pixel^{-1} s^{-1}. This is in agreement with the constant biasing measurements, where the sensor with the higher dose also shows less fake-hit rate for moderate temperatures. The downwards trend can, however, not be explained by imperfect threshold tuning as there the mean threshold is also falling slightly with increasing temperature and usually threshold and fake-hit rate anticorrelate. For the sensor with the highest non-ionizing dose of 10^{15} 1 MeV n_{eq} cm^{-2}, it could possibly improve understanding of both the threshold and the fake-hit rate curve, if the measurement is repeated with a decreased temperature step size of for example 1 °C. The high fake-hit rate at 30 °C shows again that the operating point of this chip at this specific temperature is not chosen well.

8.3 Energy Calibration

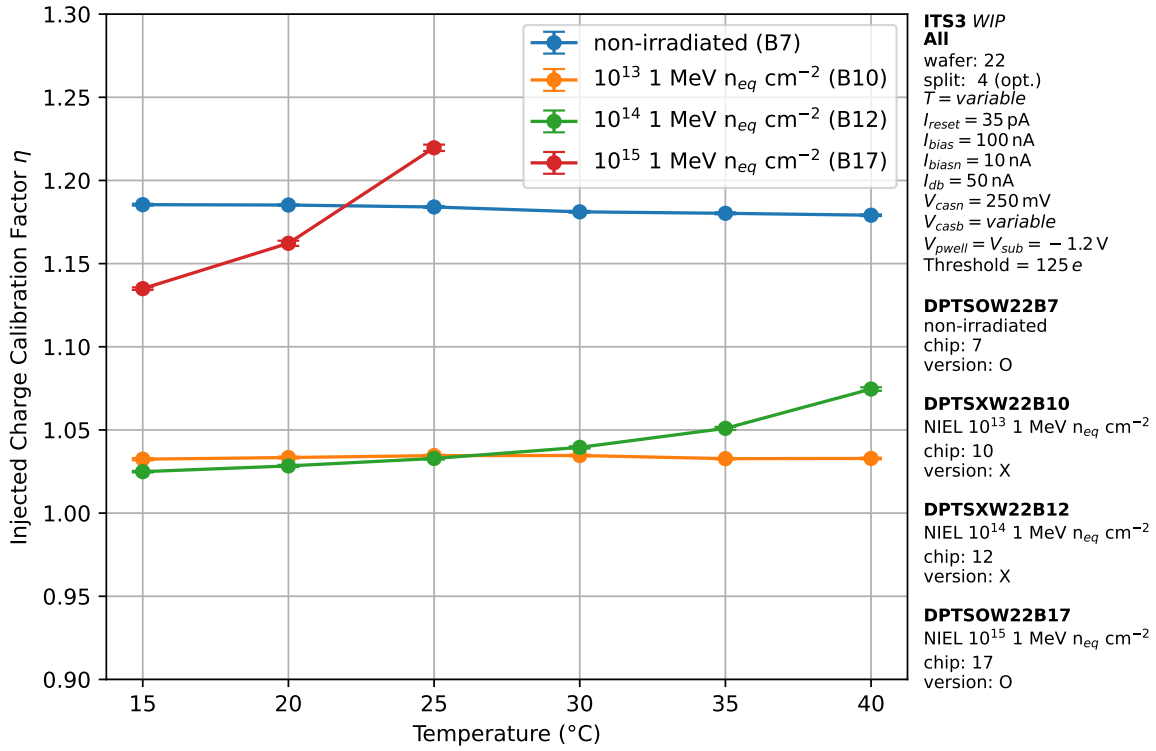


Figure 8.7: Injected charge calibration factor in dependency of the temperature for different dose levels of non-ionizing radiation.

The injected charge calibration factor was tested to be mostly independent of biasing parameters including the back bias V_{bb}. The main contribution to varying injected charge calibration factors is chip-to-chip variation of different chips. This can however not be disentangled from effects of non-ionizing radiation, because due to the irradiation process it is not possible to characterize the chip before irradiation. Thus, the information value of chip-to-chip comparisons in this section is limited. Figure 8.7 shows temperature curves for the injected charge calibration factor for the four chips from the previous chapters. In order to be able to take properly decodable scans, five pixel have to be masked for the $10^{14}\,1\,\mathrm{MeV}\ \mathrm{n}_{eq}\ \mathrm{cm}^{-2}$ chip and one pixel has to be masked for the $10^{15}\,1\,\mathrm{MeV}\ \mathrm{n}_{eq}\ \mathrm{cm}^{-2}$ chip.

The injected charge calibration of the non-irradiated chip is fairly temperature-stable. At 15 °C, the injected charge calibration factor is 1.185 ± 0.001. It drops by about 0.6 % to 1.179 ± 0.001, when heating the chip up to 40 °C. For the $10^{13}\,1\,\mathrm{MeV}\ \mathrm{n}_{eq}\ \mathrm{cm}^{-2}$ chip, the injected charge calibration factor increases from 1.032 ± 0.001 to 1.033 ± 0.001, which means a relative increase of less than 0.1 %. Increasing the irradiation level by another factor of 10 to $10^{14}\,1\,\mathrm{MeV}\ \mathrm{n}_{eq}\ \mathrm{cm}^{-2}$, the injected charge calibration factor is not linear anymore. It is measured to be 1.025 ± 0.001 at 15 °C increasing exponentially up to 1.075 ± 0.002 at 40 °C.

Thus, a total increase of 0.050 ± 0.003 over the range of 25 K is observed. Since threshold scans only work reliably up to 25 °C on the 10^{15} 1 MeV n_{eq} cm^{-2} chips, also the injected charge calibration factor was evaluated only up to this temperature. At 15 °C, the injected charge calibration factor is measured as 1.135 ± 0.001. Increasing the temperature by 5 K only, rises the injected charge calibration factor already up to 1.162 ± 0.002. Another 5 K will increase the injected charge calibration factor to 1.220 ± 0.002. Over a temperature range of 10 K, the factor increased by 0.058 ± 0.003, showing a much larger temperature dependency than chips irradiated to lower levels of non-ionizing radiation.

To sum up, the injected charge calibration can be considered independent of the temperature for practical purposes in a temperature range 15 °C to 40 °C and $\leq 10^{13}$ 1 MeV n_{eq} cm^{-2}. At higher NIEL-levels, the temperature effect becomes non-negligible and has to be considered, when taking any data that requires an injected charge calibration. Concerning ALICE 3, the temperature measurement range should be increased down to −25 °C or lower, in order to have reliable results also at the expected temperatures of operation. Even though the final chip for the ITS3 and the ALICE 3 Vertex Detector will likely not have direct energy resolution capabilities for the sake of reduced power consumption as in the ITS2 [Abe+14], this result is important, as it also affects the threshold tuning of the sensor. Considering the expected NIEL doses for both use cases, this behavior will most likely not be an issue for the ITS3, but for ALICE 3 only.

8.4 Efficiency

In order to study the efficiency under influence of non-ionizing radiation, the four same chips, including one reference, from the previous studies are tested in beam. As in section 7.8, the targeted efficiency is 99 %. The campaign took place at CERN PS in July 2022. The beam consists of positive hadrons with 10 GeV/c momentum. In addition to beam data, threshold and fake-hit rate scans as well as decoding calibrations are taken in-situ. The back bias V_{bb} is chosen to be −2.4 V. As for all irradiated chips, $I_{\mathrm{reset}} = 35$ pA and $I_{\mathrm{db}} = 50$ nA are set. V_{casn} is tuned to 350 mV prior to the measurements. For each chip, a range of different V_{casb}, and thus also thresholds, is scanned over taking 10 000 events per setting. This is done to be able, to estimate the margin of ideally > 99 % efficiency with a tolerable fake-hit rate. Additionally to the three NIEL levels, one non-irradiated reference sensor is shown. This is the same dataset as for the reference sensor in the previous chapter.

The results are shown in figure 8.8. Without exception, all sensors show fake-hit rates at the lower sensitivity limit down to a threshold of 125 e. Thus, the fake-hit rate is not strongly affected by the damage induced from non-ionizing radiation, which reinforces results

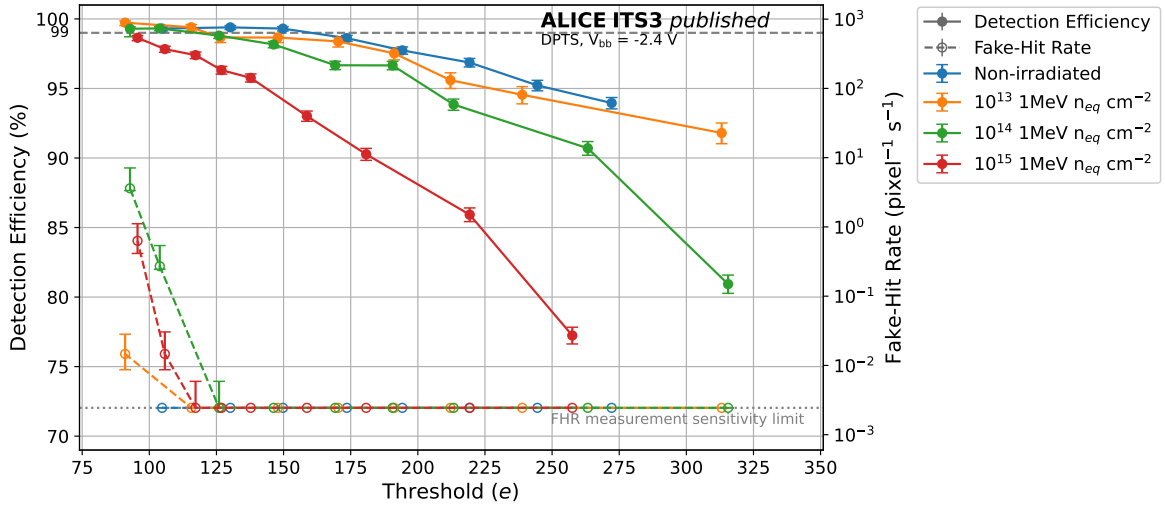


Figure 8.8: Efficiency and fake-hit rate measured in-situ at at beam test for different levels of non-ionizing radiation. The data was taken at CERN PS in July 2022.

from section 8.2.2. Other than that, the efficiency drops. With the sensor irradiated up to 10^{13} 1 MeV n_{eq} cm^{-2}, it is still possible to reach above 99 % efficiency while measuring a fake-hit rate at the sensitivity limit. This is an important result in view of the ITS3 as this NIEL dose is the expected value for the non-ionizing radiation load during its expected run time. The efficiency at higher thresholds is degraded slightly. Values higher than 99 % can only be reached at thresholds of about 120 e, whereas the reference sensor achieves this up to 160 e. The radiation damage has thus reduced the operational margin of the sensor. The sensor irradiated up to 10^{14} 1 MeV n_{eq} cm^{-2} does reach more than 99 % efficiency only at the cost of increased fake-hit rate in the order of at least 10^{-1} $pixel^{-1}$ s^{-1}. With a NIEL dose of 10^{15} 1 MeV n_{eq} cm^{-2}, 99 % efficiency is not reached anymore at any threshold. However the degradation of efficiency is not very severe, so that a maximum of 98.2 % is still achieved with a fake-hit rate below 1 $pixel^{-1}$ s^{-1}.

This does not yet meet the requirements for ALICE 3, where the expected dose is another factor of 10 higher than the dose this chip has received. The ALICE 3 Vertex Detector will likely not be cooled to +20 °C only, but possibly to temperatures in the order of −25 °C [Col22a]. This is expected to increase the efficiency at given NIEL dose and enables also chips with higher doses to be operated (see section 8.5 and [Spi05]). Furthermore, this results is an important step on the way towards designing chips more radiation hard than the DPTS, which eventually can withstand 10^{16} 1 MeV n_{eq} cm^{-2} or more potentially even at room temperature.

8.5 Studies on Sensors with Higher Neutron Doses

With increasing NIEL dose the leakage current of the sensor is expected to increase (cf. section 3.3.2). This can be compensated for by either decreasing the temperature or increasing I_{reset}. In laboratory tests, both $2 \cdot 10^{15}\,1\,\text{MeV}\ \text{n}_{eq}\ \text{cm}^{-2}$ chips are tested with the minimum achievable temperature of 14 °C. Then I_{reset} is increased and the analog and CML output are checked with an oscilloscope. It was not possible, to increase I_{reset} enough to get a reasonably looking signal on either channel. This shows as either no CML output at all, uncorrelated analog and CML outputs or very short ToT in $\mathcal{O}(0.1\,\mu\text{s})$, being about 100 times shorter than usual ToT (cf. figure 5.7). With the DAQ board and proximity, the maximum current is limited to $I_{\text{reset}} = 70\,\text{pA}$. The board acts as a current sink here. When setting the pad voltage to 0 V, the maximum potential difference is achieved and thus the maximum current is flowing.

One approach, to get the chips operational is to further increase I_{reset}. The current can be increased by breaking the connection between proximity and carrier "reverse-biasing" the corresponding `CE_PMOS_AP_DP_IRESET` pad of the chip. Therefore, the positive output of a power supply channel is connected to ground of the chip. The negative output is connected to the carrier pad trough a *Keysight 34465A* multimeter for current measurement. When increasing the output voltage, the pad is in fact pulled to a higher potential difference with respect to the positive supply voltage, therefore increasing I_{reset} above 70 pA. However, this is only a workaround rather than a real solution, as the chip is not designed for this operation and might be damaged by this. In tests, I_{reset} was increased up to 133 pA. Judging from the measurements taken, this did not damage the chip. Figure 8.9 shows the analog and digital waveforms of one of the $2 \cdot 10^{15}\,1\,\text{MeV}\ \text{n}_{eq}\ \text{cm}^{-2}$ DPTS when pulsing the monitor pixel. The chip is operated at +14 °C and with $I_{\text{reset}} = 133\,\text{pA}$. The other chip parameters are $V_{\text{bb}} = -1.2\,\text{V}$, $V_{\text{casb}} = 170\,\text{mV}$, $V_{\text{casn}} = 140\,\text{mV}$, $I_{\text{bias}} = 300\,\mu\text{A}$, $I_{\text{biasn}} = 30\,\mu\text{A}$ and $I_{\text{db}} = 200\,\mu\text{A}$, and thus all in the normal operating range. The analog signal looks as expected, the ToT is in a reasonable range and analog and CML signal are well correlated. No threshold scan is done here, as the operation with increased I_{reset} requires operation with the DPTS BoB, on which threshold scans are not easily doable. It is however expected that such outputs allow a threshold to be determined, when using another setup.

The other option of lowering the operation temperature at I_{reset} within the specifications is also scoped. Therefore, the chip is operated in a climatic chamber of the CERN *Quality Assurance and Reliability Testing (QART)* laboratory of the EP-DT-DD section. The climatic chamber can lower the temperature down to −70 °C while controlling the humidity inside such that no condensation will occur. Only the carrier board is placed inside the box to not

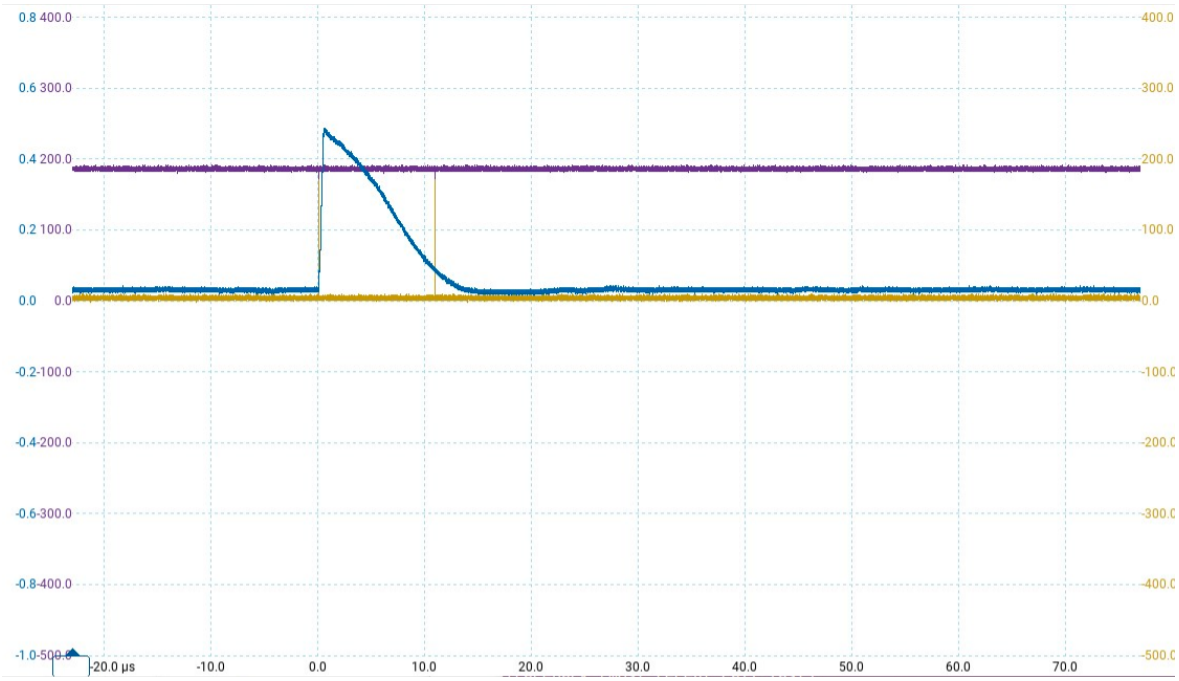


Figure 8.9: Waveform of a $2 \cdot 10^{15}$ 1 MeV n_{eq} cm^{-2} DPTS at +14 °C after pulsing the analog monitor pixel. The time base is set 10 µs/div, the CML output is set to 100 mV/div and the analog output is set to 200 mV/div.

entangle the results with temperature dependency of components on the DAQ or proximity board. Therefore, custom PCIe extension cords are used. They were validated beforehand giving comparable results with respect to direct connection of the carrier card to the proximity board.

The result of a threshold scan at 0 °C is shown in figure 8.10. At this operating point, the fake-hit rate is at lower sensitivity limit. However decreasing the threshold further does not work as it leads to unreasonable S-curves, where the detected number of hits seems uncorrelated to the injected charge from a certain pulsing voltage V_{h} on. In order to try to lower the the threshold the temperature is decreased to −10 °C. Now, a mean threshold of 123.8 e is reachable, whereas I_{reset} could even be lowered to the nominal value of 35 pA for irradiated sensors. The threshold histogram is depicted in figure 8.11. The fake-hit rate is determined as $(6.83\ ^{+6.70}_{-0.43}) \cdot 10^{-1}\,\mathrm{pixel}^{-1}\,\mathrm{s}^{-1}$ at this point.

At this operating point it seems reasonable to measure a ^{55}Fe spectrum to measure the energy resolution and to test the sensor in-beam in order to determine the efficiency. However, as of writing, there is no ^{55}Fe source available at CERN that is classified to be operated under 0 °C for an extended amount of time. Another source is needed for this. Testing the chip in-beam is even more complicated, since the climatic chamber can not be used in the beam test area. There are alternatives, such as replacing the water in the water cooler by silicon

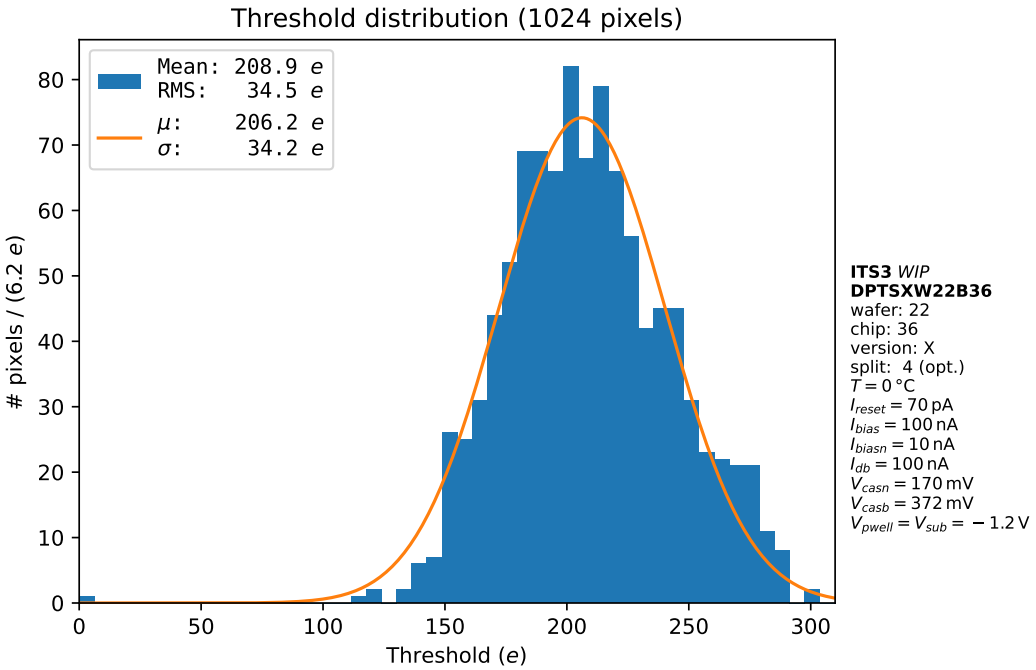


Figure 8.10: Threshold scan of a DPTS at $2 \cdot 10^{15}$ 1 MeV n_{eq} cm^{-2} and 0 °C.

oil while flushing the sensor environment with nitrogen to displace air humidity and avoid condensation. In view of ALICE 3 such techniques should be developed to be able to test prototypes far below room temperature.

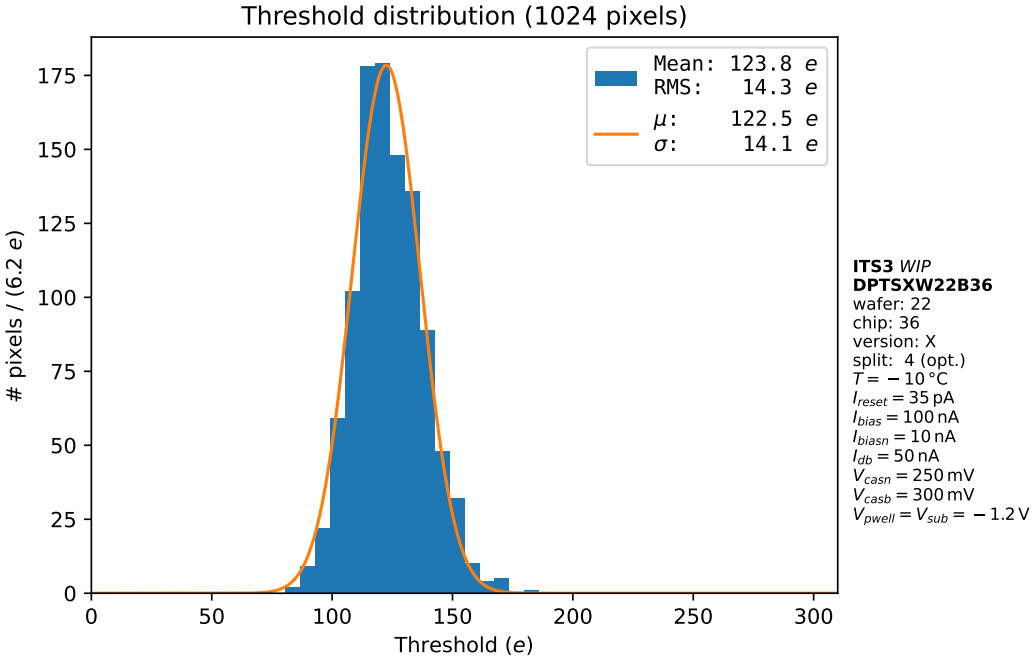


Figure 8.11: Threshold scan of a DPTS at $2 \cdot 10^{15}$ 1 MeV n_{eq} cm^{-2} and −10 °C.

Similar results have been achieved at $-20\,^{\circ}\mathrm{C}$. The histogram is attached in figure C.24 and the threshold mean calculates as $145.2\,e$. Between these two points with same biasing parameters, the threshold is rising when lowering the temperature. This is in line with results from section 8.2, where lowering the temperature always led to decreased thresholds. The fake-hit rate is measured as $(1.90\ ^{+1.77}_{-0.22}) \cdot 10^{-1}\,\mathrm{pixel}^{-1}\,\mathrm{s}^{-1}$, so a bit lower as compared to $-10\,^{\circ}\mathrm{C}$, which can be explained by the increased threshold.

Two more temperature steps are done at $-40\,^{\circ}\mathrm{C}$ and $-70\,^{\circ}\mathrm{C}$, just to push the sensor to its potential limits. Exemplary S-curves of the DPTS at $-40\,^{\circ}\mathrm{C}$ are shown in figure C.25. No proper operating point is found given the relatively short amount of time available.

Due to lack of time at the climatic chamber, a quite coarse temperature stepping was chosen. It would be of interest to study the range around $-20\,^{\circ}\mathrm{C}$ to $-40\,^{\circ}\mathrm{C}$ in a finer step size in order to study how and why the chip stops working and if it can be compensated for by tuning certain parameters. On the other hand, future tests in the climatic chamber should foresee more time at single temperature steps in order to run more extensive scans such as measuring the threshold and fake-hit rate over a wider range of V_{casb}. Furthermore, higher doses of non-ionizing radiation, such as $5 \cdot 10^{15}\,1\,\mathrm{MeV}\ \mathrm{n}_{eq}\ \mathrm{cm}^{-2}$, $10^{16}\,1\,\mathrm{MeV}\ \mathrm{n}_{eq}\ \mathrm{cm}^{-2}$ and possibly even higher should be tested. Nevertheless, this first campaign of measuring DPTS at temperatures of $0\,^{\circ}\mathrm{C}$ and lower provides valuable first studies on the non-ionizing radiation hardness of MAPS in *TPSCo.* 65 nm CMOS technology at doses towards the ALICE 3 Vertex Detector.

8.6 Summary

The non-ionizing radiation hardness is tested with neutrons. Studies in this thesis yield following key results:

- The fake-hit rate becomes more sensitive to a shift of temperature, as the non-ionizing radiation dose increases. The fake-hit rate tends to increase with increasing temperature. The increase of fake-hit rate per temperature increases with non-ionizing radiation load.
- The threshold decreases with increasing temperature. An increased level of non-ionizing radiation dose makes the threshold more sensitive to temperature changes.
- Timing parameters of the decoding calibrations are temperature-sensitive. Non-ionizing radiation does not affect the temperature coefficients of the timing parameters.
- At constant threshold, the fake-hit rate is not temperature-dependent. This indicates that the increase in fake-hit rate is only a consequence of a shifted threshold.

- At 10^{15} 1 MeV n_{eq} cm^{-2}, a DPTS stops working above 25 °C.
- The injected charge calibration factor is temperature-stable for low non-ionizing doses, but increases with temperature for doses above 10^{13} 1 MeV n_{eq} cm^{-2}.
- At ITS3 non-ionizing doses, a DPTS is operable at +20 °C with > 99 % efficiency and very low fake-hit rate.
- At ALICE 3 non-ionizing doses, a DPTS is not operable at room temperature. At $2 \cdot 10^{15}$ 1 MeV n_{eq} cm^{-2}, a DPTS works only with temperatures below 0 °C or with reset current increased to values out of specifications.

To conclude, the non-ionizing radiation hardness of the *TPSCo.* 65 nm CMOS technology at ITS3 levels is shown. It has to be kept in mind that cooling the chip to below-zero temperatures is an option in ALICE 3. Therefore, in view of ALICE 3, further studies especially at sub-zero temperatures are needed.

9 Conclusion and Outlook

With the installation of the ALICE ITS2 during LHC Long Shutdown 2, the ALICE experiment is replacing older silicon detector technologies with state of the art MAPS produced in the *TowerJazz* 180 nm process. It is envisaged to upgrade the ITS2 to the ITS3 in LHC Long Shutdown 3. The technology will be changed to the *TPSCo.* 65 nm process. In the R&D effort for this project, a first series of prototype sensors was produced. This thesis studied several aspects of the radiation hardness of the Digital Pixel Test Structure (DPTS). In order to evaluate the radiation hardness, irradiation campaigns were carried out. X-rays are used to test the DPTS in view of its hardness against ionizing radiation, while neutrons are used to study the hardness against non-ionizing radiation.

The DPTS irradiated to ionizing doses expected during the lifetime of the ITS3 is characterized in depth. It can be observed that ionizing radiation leads to an increase of the fake-hit rate of the sensor, as well as it causes a decrease in the mean threshold. By tuning certain biasing parameters of the chip, it is possible to keep the threshold constant while irradiating the chip to 200 kGy over a duration of a few hours only. Beam test results reveal that 99 % detection efficiency are easily reachable at ITS3 ionizing radiation doses, while maintaining a low fake-hit rate. Annealing of the sensor at room temperature will lead to fast decrease of fake-hit rate in the first hours after end of irradiation. Also the threshold recovers to higher values again, but on a longer timescale of weeks only. At ionizing radiation levels higher than expected for the ALICE 3 Vertex Detector, the DPTS is still able to reach close to 99 % detection efficiency with tolerable fake-hit rate. However, in order to be able to achieve this, two months of annealing are needed here. In ALICE 3, the dose rate will be much lower than in these tests, such that annealing effects will play a bigger role. Lastly, the ionizing radiation hardness to levels of the ITS3 is shown. In view of ALICE 3, further studies are needed, but these results give a hint that the required ionizing radiation hardness could be reachable with this technology.

Under the influence of non-ionizing radiation damage, it is observed that the temperature dependency of the threshold is changing. The threshold becomes temperature-sensitive with increasing non-ionizing radiation dose. The fake-hit rate is measured at different temperatures and non-ionizing radiation doses with a tuned threshold at every point. There, the fake-hit

rate is constant, which hints that the noise in the sensor is not a direct consequence of the biasing parameters, but of the applied threshold. At doses expected for the ITS3, more than 99 % detection efficiency are reached at a very low fake-hit rate and 20 °C. At expected doses of ALICE 3, the chip is not operable at room temperature. Studies at decreased temperature hint that an operation might be possible there. Further studies are needed and ongoing. The highest operable non-ionizing dose at room temperature is 10^{15} 1 MeV n_{eq} cm^{-2}, where close to 99 % detection efficiency are reached with a moderate fake-hit rate. The radiation hardness at doses of the ITS3 is shown. To this point, this can not be shown for ALICE 3 non-ionizing radiation doses. As sub-zero degrees cooling is a viable option in ALICE 3, further studies in this direction should and will be carried out. In particular, it will be necessary to study the efficiency of sensors at more than 10^{15} 1 MeV n_{eq} cm^{-2} and decreased temperature.

It can be concluded that th DPTS test structure produced in the *TPSCo.* 65 nm CMOS process is sufficiently radiation hard in both ionizing and non-ionizing radiation scenarios needed for the ITS3 project. Looking forward to the ALICE 3 Vertex detector, it is too early to give a final statement on the required radiation hardness of this technology. However, first results indicate that the necessary ionizing radiation hardness is reachable even at room temperature. The non-ionizing radiation hardness is, with this tested structure, not achieved at room temperature. Anyhow, this does not disqualify the *TPSCo.* 65 nm CMOS process as technology node for ALICE 3, as important results, especially at lower temperatures are still missing. Lastly, this was only the first iteration of test structures and with knowledge gained also from other test structures of this submission, further improvements of the sensor design itself are also possible.

A Additional Details on the Beam Test Setup

The results of this work were obtained at the CERN PS and DESY II [Die+19] accelerators. Both facilities provide a beam of minimum ionizing particles. In detail, the PS beam will generate a secondary beam of charged hadrons (mostly protons and pions) with 10 GeV or 12 GeV momentum and selectable polarity from a primary proton beam and a target. At the DESY II accelerator, electrons are accelerated. A secondary beam will be generated by using the bremsstrahlung from the primary beam in the synchrotron. The synchrotron radiation will produce electron-positron pairs in a target. With magnets, the electron/positron momentum and polarity can be selected. [Die+19] The momentum ranges from 1 GeV to 6 GeV, while 3.4 GeV or 5.4 GeV were used here.

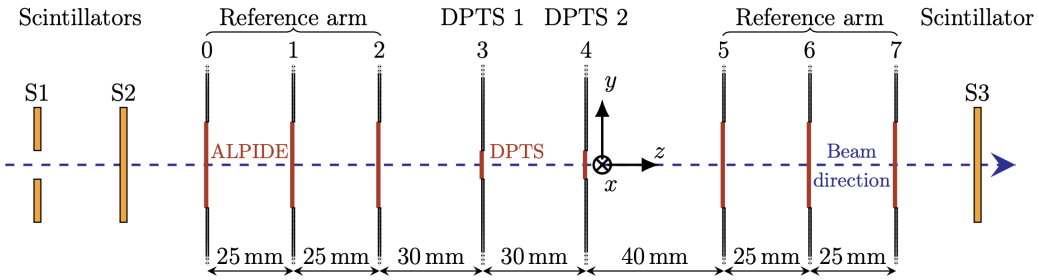


Figure A.1: Schematic view of the telescope planes used for the beam test setup. Taken from [Agl+23, Fig. 15].

The device under test (DUT) is placed inside a telescope together with six reference planes equipped with ALPIDE chips. An overview on this setup is given in figure A.1. The ALPIDE planes cover a much larger area of 29 mm × 27 mm compared to the 480 µm × 480 µm area of the DPTS planes. If one triggered the DPTS readout based on hits in the ALPIDE planes, just by geometry most of the events would not have any hits in the DUT plane. For this reason, a second DPTS is added in the proximity of the DUT plane. In the schematic, these planes are called DPTS 1 and DPTS 2. In the first order, it does not matter whether the DUT or the trigger plane comes first with respect to the beam. However, since especially previously irradiated chips are expected to show strong temperature dependency in their operation, an aluminium cooling jig is placed behind the PCB of the DUT. To minimize the material between trigger and DUT, it is best to place the trigger DPTS upstream with respect

to the DUT. The DUT is cooled to 20 °C. The trigger DPTS is mounted on a combination of two *ZABER* linear moving stages to achieve movement in XY-direction. This DPTS will be operated with nominal parameters, easily achieving $> 99\,\%$ efficiency with a tolerable fake-hit rate at ambient temperature in a closed box[1].

All telescope planes are thus read out only when there has been a hit in the trigger plane. Technically, this is achieved by triggering the oscilloscope on the rising edge of the channel connected to the non-inverting CML output of the trigger DPTS. This will automatically also trigger the capture of the non-inverting CML output of the DUT. The whole trigger and busy logic is shown in figure A.2, whereas the connections for regular data taking are marked in black and green. Both of those chains will ensure synchronization of all hits in all ALPIDE and DPTS planes. Moreover, the oscilloscope is configured in a way that the arbitrary waveform generator (AWG) sends a pulse if the oscilloscope has been triggered. This signal is used to trigger the readout of all the ALPIDE planes, whereas the first plane is triggered by the oscilloscope, the second plane is triggered by the trigger output of the first plane and so on. A busy chain is established in the logically opposite direction, whereas the busy output of the first plane is connected to the auxiliary input (AUX) of the oscilloscope. The oscilloscope is configured such that it acts as a veto for the trigger. In other words, the oscilloscope will not accept a new trigger from the trigger device as long as at least one ALPIDE plane is not finished transmitting data. It is worth mentioning that the trigger in- and outputs of the DAQ boards of the DPTS planes remain unconnected. This is because the data acquisition on these planes is not done via the DAQ boards, but by the oscilloscope. This however has to be changed, when in-situ measurements of the threshold and the fake-hit rate are supposed to be taken. In that case, the trigger output of the DUT DAQ board is fed into the AUX input of the oscilloscope, as it is in the laboratory measurements. This connection is shown in blue.

To align the telescope with respect to the beam, it is favorable to have a larger trigger area, in order to see correlations of the detector planes more easily. In this case, a plastic scintillator in combination with a photomultiplier tube (PMT) is used as the trigger device. The active area of these scintillators is roughly $2\,\text{cm} \times 2\,\text{cm}$. The scintillator can be upstream or downstream from the DUT plane and both configurations have been used in the beam tests that were carried out. Control and power for the PMTs is provided by a custom-made trigger board. This board is connected to the data taking PC via USB and will provide correct voltages to set gain and threshold. The board will then also act as the master of the trigger chain and will terminate the busy chain. Two more PMTs are shown in the schematic view. These

[1] Temperatures in the beam test box have been observed to exceed 30 °C by heat dissipation of all the electric components.

can be used as a backup in case triggering on the DPTS does not work or if an uncorrelated time reference for time resolution measurements is needed. The logic of the trigger board will be configured such that a signal is considered the trigger, if the upstream and downstream PMTs both show a signal. The upstream PMT with a hole in it is used as a veto to reduce the number of events without any hit in the DPTS planes. In order to achieve an alignment between the DPTS planes and the PMT with a hole, this PMT is also placed on a remotely controllable XY-stage.

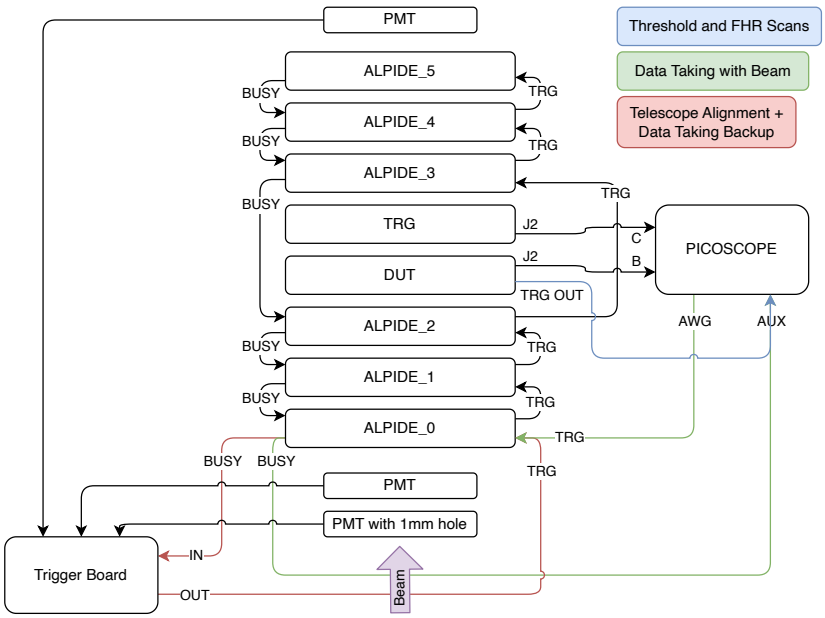


Figure A.2: Schematic of trigger and busy chain between all ALPIDE and DPTS planes as used in beam tests. Connections in black are always connected. The configuration in blue is used for in-situ threshold and fake-hit rate measurements and the green configuration is used for datataking with the DPTS as trigger. The red configuration is used to align the telescope with respect to the beam as well as it can be used as backup, if triggering on the DPTS trigger device is not possible.

In figure A.2, it can also be seen that the inverted CML outputs on J3 of the carrier PCB remain unconnected. This is due to the fact that, in contrast to the laboratory measurements, two DPTS have to be read out by the same oscilloscope. All available oscilloscopes for this purpose do have a sufficient amount of at least four channels. However, when using more than two channels on any of those oscilloscopes, the sampling rate will be cut in half. In order to keep some margin, it is preferred here to waive recording the full differential signal. Instead, during beam tests, there is no zero suppression while taking data and the complete waveforms are saved. Although this heavily increases the amount of saved data by orders of magnitude, this is done as it enables data taking without biasing the data. When analyzing the data, one can choose the threshold in the waveforms to be any value in the middle of

that range. Usually, 30 ADC units are chosen here, but in case of problems, this value can still easily be changed as whole complete waveforms were saved in the first place.

EUDAQ2 [Ahl+20] is used as data acquisition framework. A set of custom-made modules, called producers, is loaded, so that *EUDAQ2* is able to read data from all telescope planes as well as other parameters, such as supply voltages, supply currents and air and cooling jig temperature. All data is stored in a special *EUDAQ2* file format. These files are later on analyzed with *Corryvreckan* [KSW19]. This framework enables the reconstruction of tracks through the telescope planes, which is necessary to calculate the sensor efficiency. Furthermore, there are modules to calculate the spatial and temporal resolution of the sensors.

B Measurement of S-Curve Noise

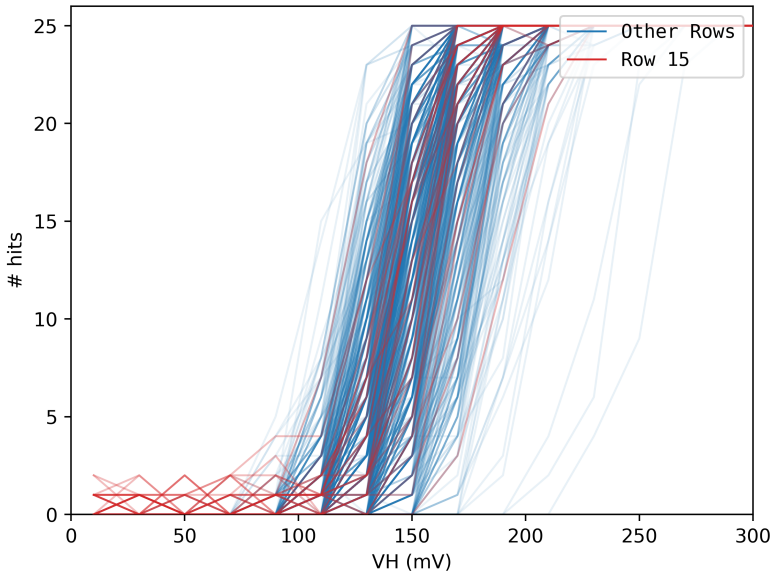
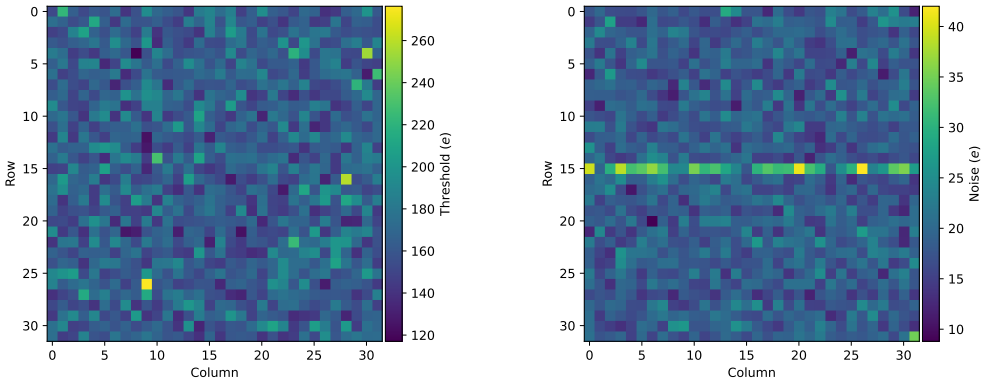


Figure B.1: S-curves of a sensor with one pixel with high fake-hit rate. The S-curves from pixels of the same row as the noisy pixel are shown in blue.

During analysis of the results of the March TID campaign, it became apparent that the S-curve noise cannot be reliably measured when there are pixel with a high fake-hit rate present in the matrix. The S-curve noise is defined as standard deviation of the derivative of a single S-curve. Thus, a particular S-curve noise can be determined for every single pixel. However, the way the threshold scans are implemented, S-curves of pixels within a row are not uncorrelated. This is due to the fact that during the scan of a row, only this row is unmasked, while all other pixels remain masked. A decoding of the hits is not done. The information about the hit position is known only by taking into consideration which pixel actually has been pulsed. In case there are fake-hits from another pixel in the same row coming in, these cannot be distinguished from real hits produced by pulsing. As the fake-hit rate of a single pixel is unrelated to the injection voltage V_{h} of another pixel, rows with this behavior can be observed as S-curves with more than 0 hits in regions of low injection charge.

Figure B.1 shows a threshold scan where exactly this happens. The S-curves of pixels from row 15 are shown in red, all other rows in blue. Regardless of the injection voltage V_{h}, there are always a few hits registered while scanning this row 15. The calculated thresholds and noises can be seen in figure B.2. In the threshold map in figure B.2a, the affected row 15 is not particularly apparent. In the S-curve noise map in figure B.2b, row 15 is however very clearly visible, showing many pixel with increased noise. Especially the pixel with high fake-hit rate (c=20, r=15) can be spotted easily.



(a) Threshold Map (b) S-Curve Noise Map

Figure B.2: Example of a threshold scan containing a pixel with high fake-hit rate. The noisy pixel has the coordinates (c=20, r=15).

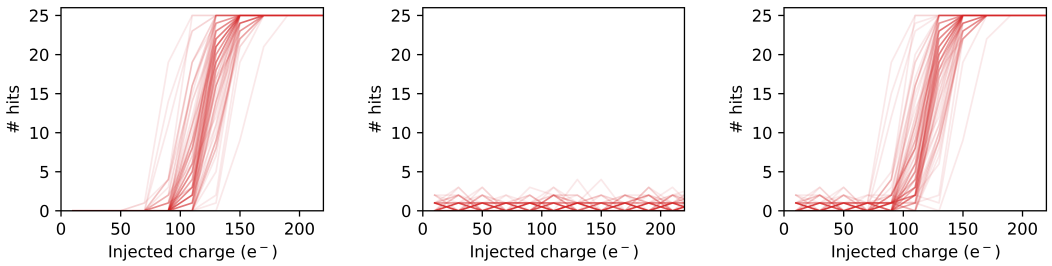
In principle, also the threshold could be influenced by an increased baseline of hits in the S-curves, as adding hits potentially shifts the mean of the S-curve derivative. Judging from the threshold map in figure B.2a, the effect should not be too large. To verify this, a quick simulation is done. Therefore, S-curves from a sensor with low fake-hit rate are added up with artificial noise in form of Poisson-distributed samples for every V_{h}. The fake-hits have to be uncorrelated with respect to each other in order to be properly described by a Poisson distribution, which is not at all obvious. For the purpose of this analysis, it is only assumed and would require detailed studies on the noise characteristics. The parameter of the Poisson-distribution calculates as

$$\lambda = \mathrm{FHR} \cdot \Delta T_{\mathrm{WF}} \cdot n_{\mathrm{inj}} \cdot 32\,\mathrm{pixel}, \tag{B.1}$$

where 32 pixel is the amount of pixel in one row. ΔT_{WF} is the length of the oscilloscope capture (cf. section 6.4). This λ is the average amount of observed fake-hits during n_{inj} injections. An exemplary calculation for $\mathrm{FHR} = 15\,\mathrm{pixel}^{-1}\,\mathrm{s}^{-1}$ delivers

$$\lambda = 15\,\mathrm{pixel}^{-1}\,\mathrm{s}^{-1} \cdot 40.02\,\mu\mathrm{s} \cdot 25 \cdot 32\,\mathrm{pixel} \approx 0.48. \tag{B.2}$$

Figure B.3a shows a normal threshold scan without presence of pixels with high fake-hit rate. Figure B.3b shows, how the S-curves would look like, if no pulsing was happening and, if there would be a moderately high fake-hit rate of FHR $= 15\,\mathrm{pixel}^{-1}\,\mathrm{s}^{-1}$ present homogeneously over all rows. This data is a Poisson-distributed sample from a random number generator. Figure B.3c then shows the sum of the real scan and the simulated noise as it would be observable in the threshold scan. It is clearly visible that a good amount of S-curves does not start at 0 anymore but have some hits always present at low V_h.



(a) Real scan (b) Simulated noise (c) Sum

Figure B.3: Influence of simulated noise on a real threshold scan. The noise is equivalent to a fake-hit rate of FHR $= 15\,\mathrm{pixel}^{-1}\,\mathrm{s}^{-1}$ with one unmasked row.

In figure B.4, results from the same threshold scan with different simulated levels of noise were analyzed with the regular algorithm to retrieve threshold and S-curve noise. On the one hand, the mean threshold remains largely unchanged in the whole range up to FHR $= 300\,\mathrm{pixel}^{-1}\,\mathrm{s}^{-1}$. Between almost no noise at $10^{-2}\,\mathrm{pixel}^{-1}\,\mathrm{s}^{-1}$ and $300\,\mathrm{pixel}^{-1}\,\mathrm{s}^{-1}$ the threshold drops by about $3\,e$. The standard deviation of the threshold increases with increasing fake-hit rate above about $10\,\mathrm{pixel}^{-1}\,\mathrm{s}^{-1}$. On the other hand, the S-curve noise increases exponentially. At a fake-hit rate of only $10\,\mathrm{pixel}^{-1}\,\mathrm{s}^{-1}$, the analyzed S-curve noise has already doubled with respect to the scan without fake-hits. Therefore, it can be concluded that threshold scans of a sensor with high fake-hit rate are still usable for the purpose of determining the mean threshold. The S-curve noise can only be determined reliably if the fake-hit rate is below $\mathcal{O}(1\,\mathrm{pixel}^{-1}\,\mathrm{s}^{-1})$, which is often not the case for freshly irradiated TID chips.

It should be mentioned here that noisy pixel affecting other pixel in the same row instead of column is a design choice of the implemented threshold scan, rather than an intrinsic feature in the sensor design. The unmasking could easily be changed to columns or diagonals in the data taking code. Then, other pixel of the same column or diagonal firing would randomly influence the S-curve of a single pixel. It is, however, not possible to unmask a single pixel only, which would solve the problem completely. If the number of pixels with high fake-hit rate is not too high, a workaround could also be to run the threshold scan three

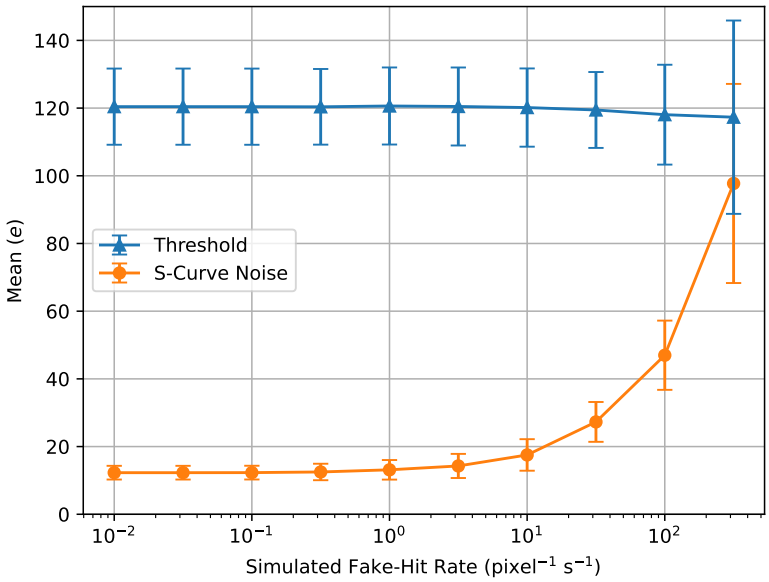


Figure B.4: Real threshold scan analyzed with different levels of simulated noise added. The errorbars are determined by the standard deviation of the underlying distribution.

times unmasking rows, columns and diagonals respectively. This would then increase the probability for a pixel to be able to record at least one S-curve which is not corrupted by noisy pixel on the same row, column or diagonal. However, this comes of course at the cost of three times increased duration for a single threshold scan. As this approach would require modifications to the data taking script, it does not help towards the recovery of S-curve noise information from the previous TID campaigns. Therefore, a detailed analysis of S-curve noise evolution under ionizing radiation cannot be done here.

C Additional Plots

C.1 Ionizing Radiation

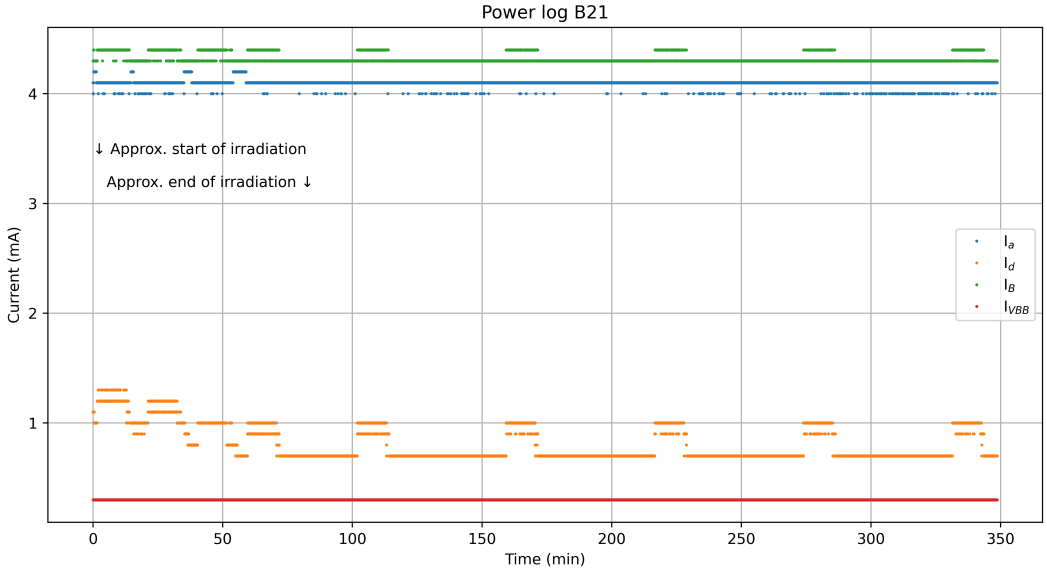


Figure C.1: Current measurement of DPTSSW22B21 during Irradiation with X-Rays.

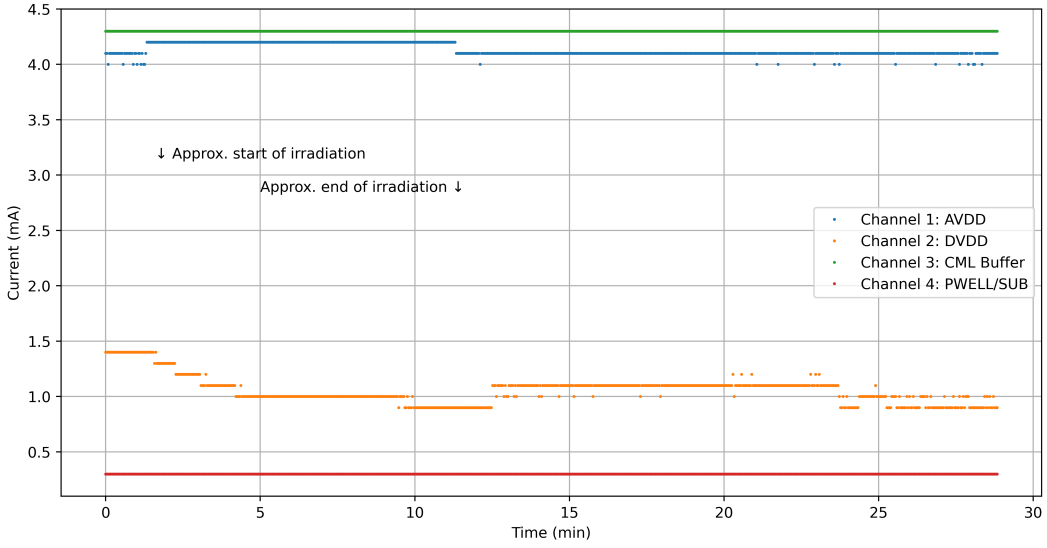


Figure C.2: Current measurement of DPTSXW22B26 during Irradiation with X-Rays.

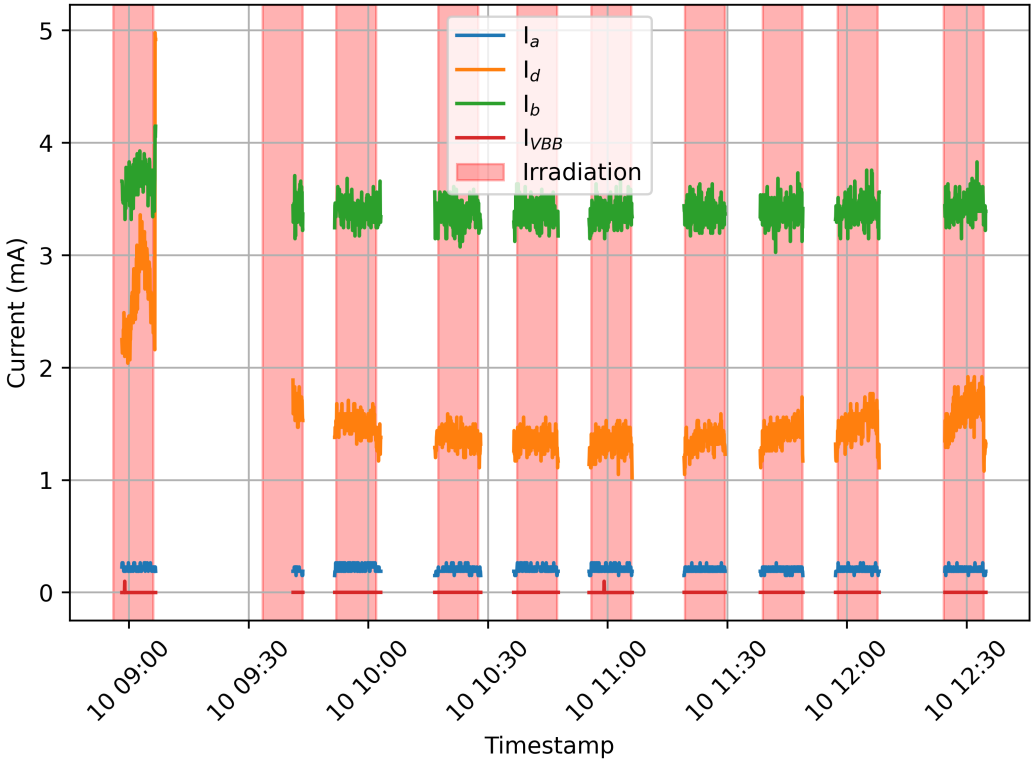


Figure C.3: Current measurement of DPTSOW22B43 during Irradiation with X-Rays. Some data in the second irradiation step is missing, because it was forgotten, to turn on the logging script.

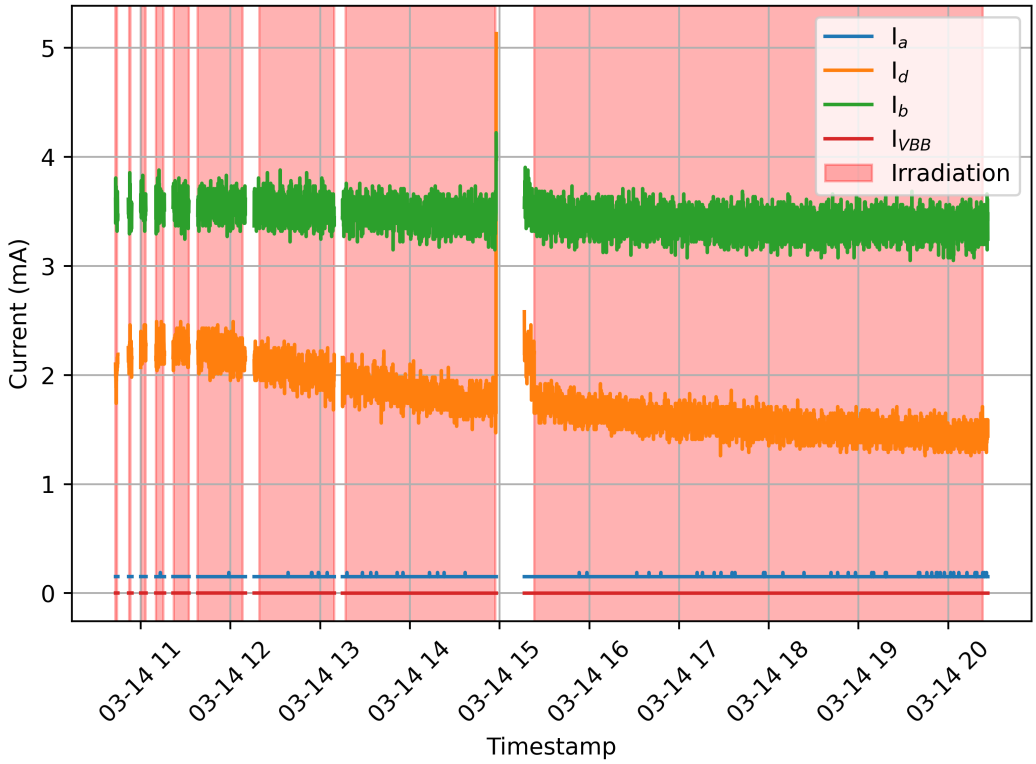


Figure C.4: Current measurement of DPTSOW22B44 during Irradiation with X-Rays.

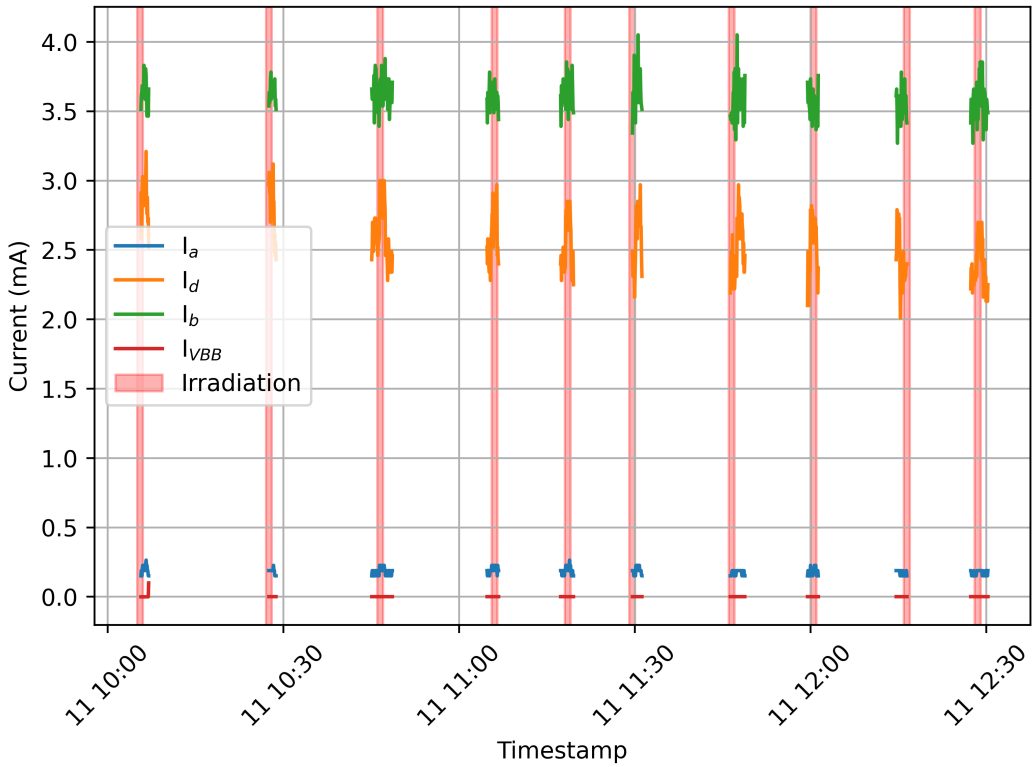


Figure C.5: Current measurement of DPTSOW22B45 during Irradiation with X-Rays.

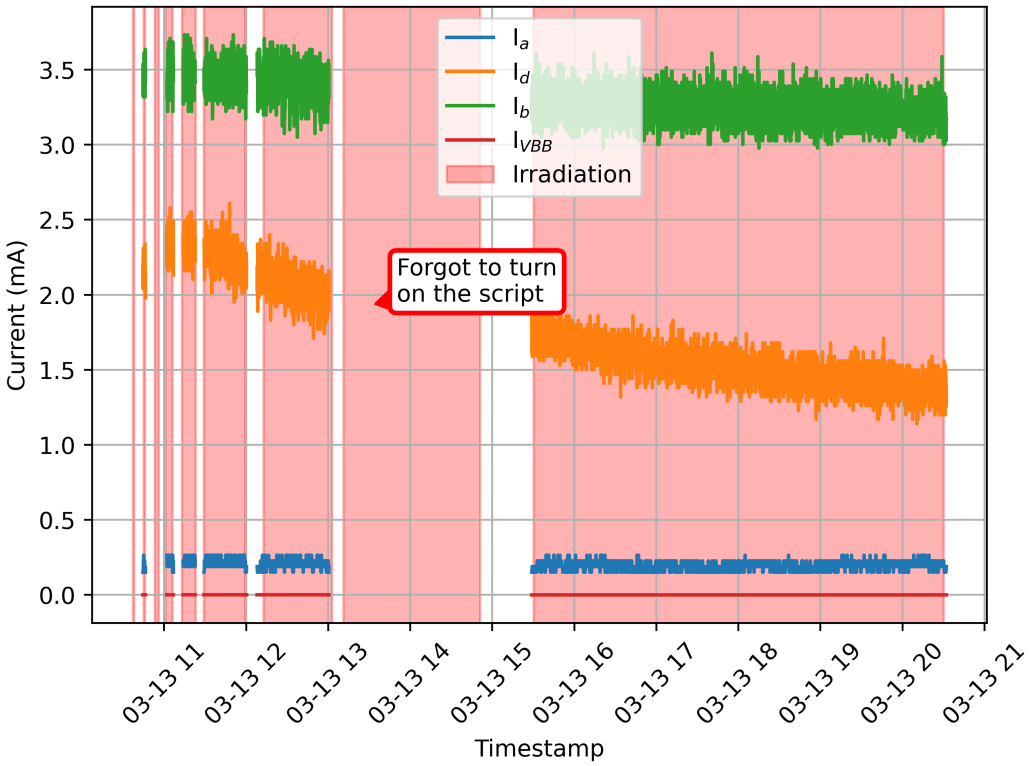


Figure C.6: Current measurement of DPTSOW22B46 during Irradiation with X-Rays.

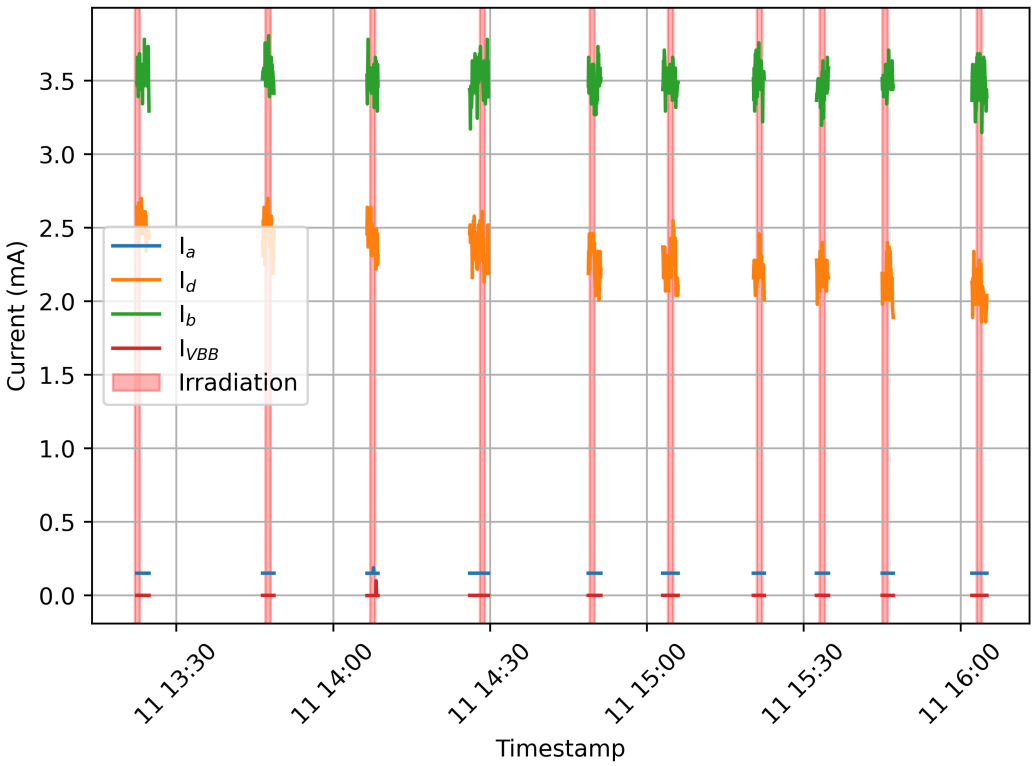


Figure C.7: Current measurement of DPTSOW22B47 during Irradiation with X-Rays.

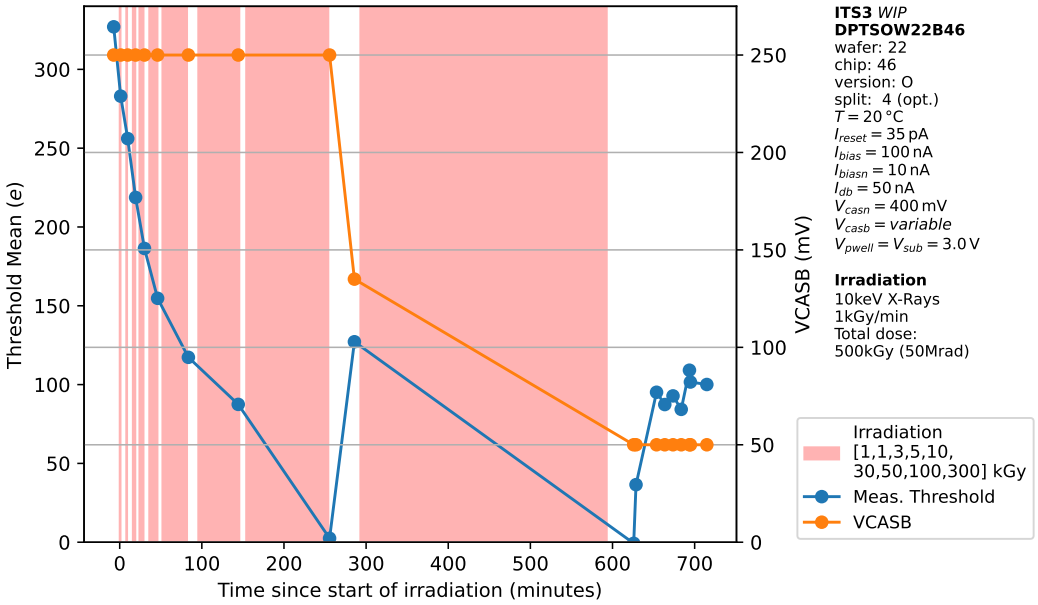


Figure C.8: Mean threshold and V_{casb} vs. time for a chip with a total dose 500 kGy. V_{casb} had to be tuned after 200 kGy in order to keep the chip operational. This was again the case after the full dose of 500 kGy.

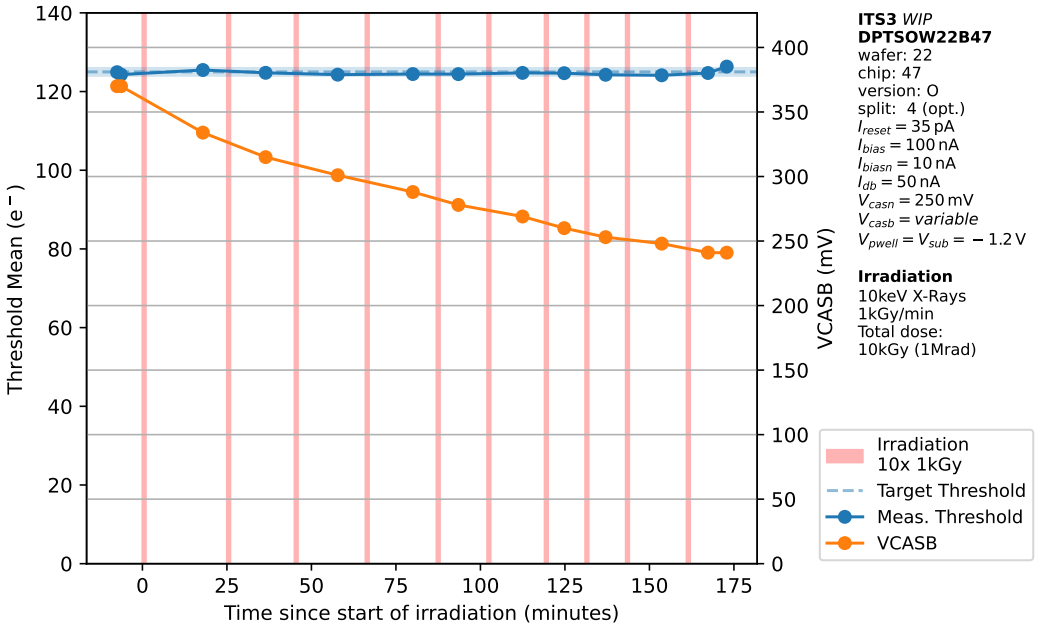


Figure C.9: Mean threshold and V_{casb} vs. time for a chip with a total dose 10 kGy. The threshold is tuned back to 125 e after every irradiation step.

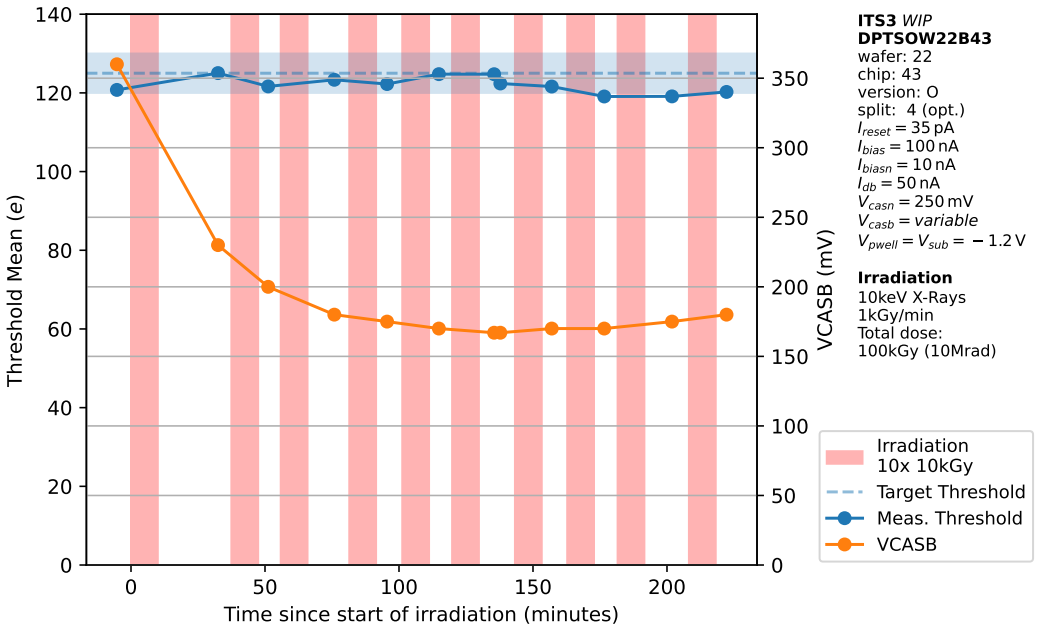


Figure C.10: Mean threshold and V_{casb} vs. time for a chip with a total dose 10 kGy. The threshold is tuned back to 125 e after every irradiation step.

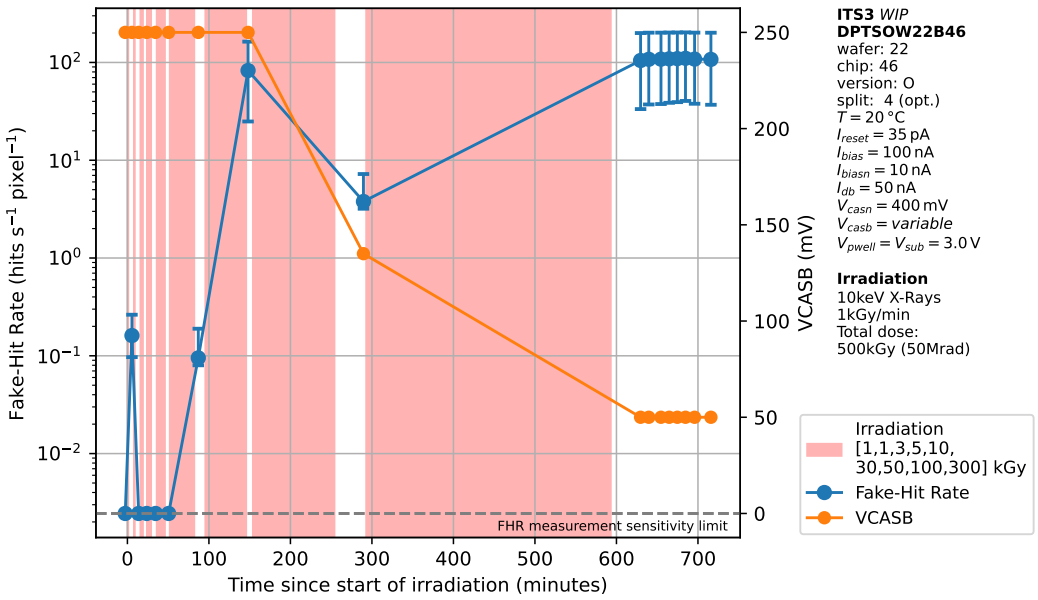


Figure C.11: Fake-hit rate and V_{casb} vs. time for a chip with a total dose 500 kGy. After 200 kGy, V_{casb} had to be tuned to keep the chip operational. This was again the case after the full dose of 500 kGy.

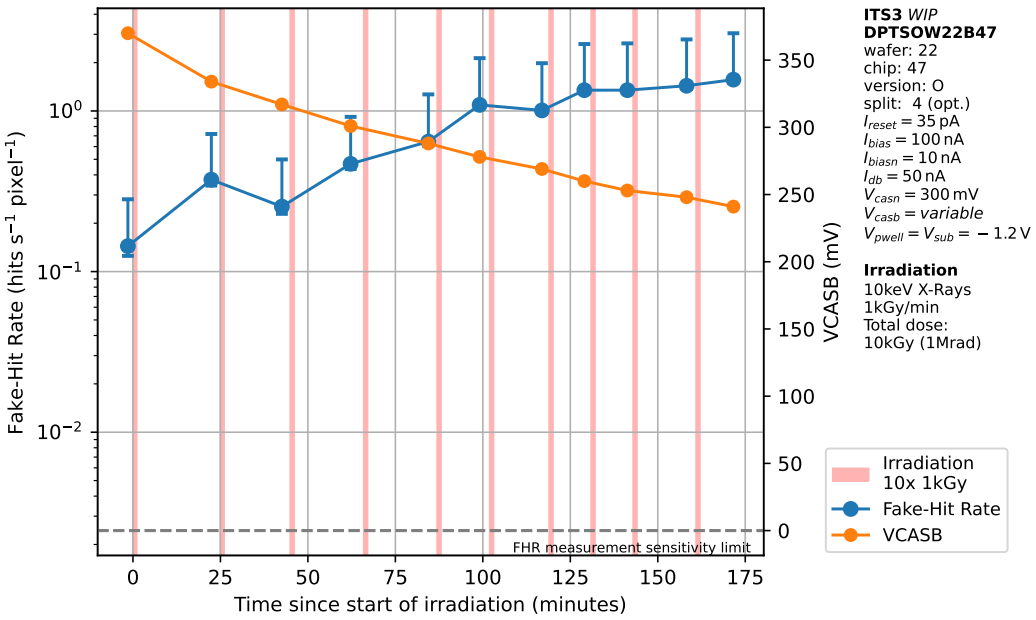


Figure C.12: Fake-hit rate and V_{casb} vs. time for a chip with a total dose 10 kGy. The threshold is tuned back to 125 e after every irradiation step.

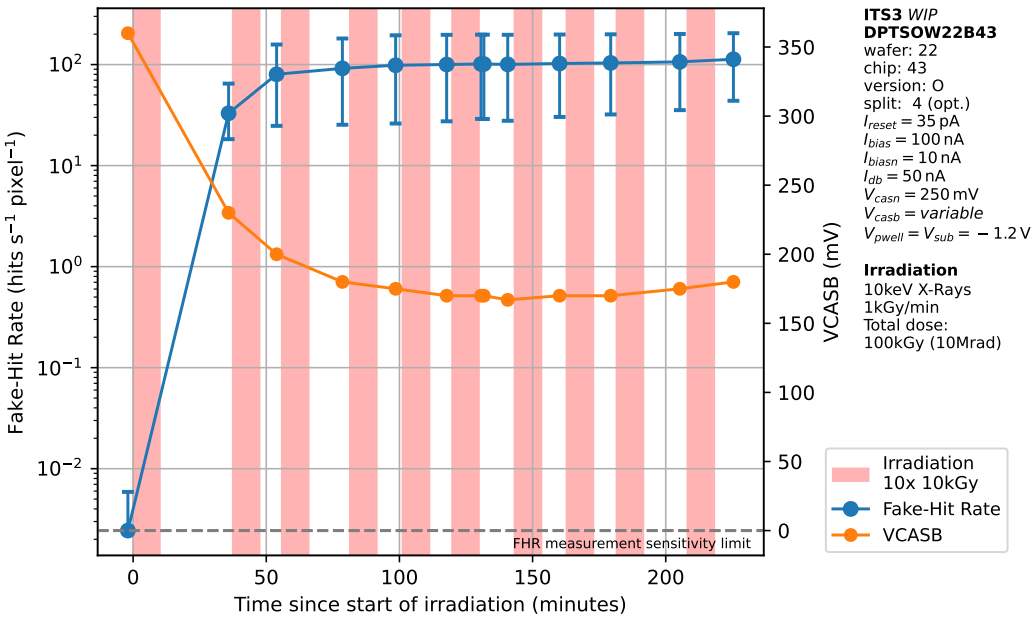


Figure C.13: Fake-hit rate and V_{casb} vs. time for a chip with a total dose 10 kGy. The threshold is tuned back to 125 e after every irradiation step.

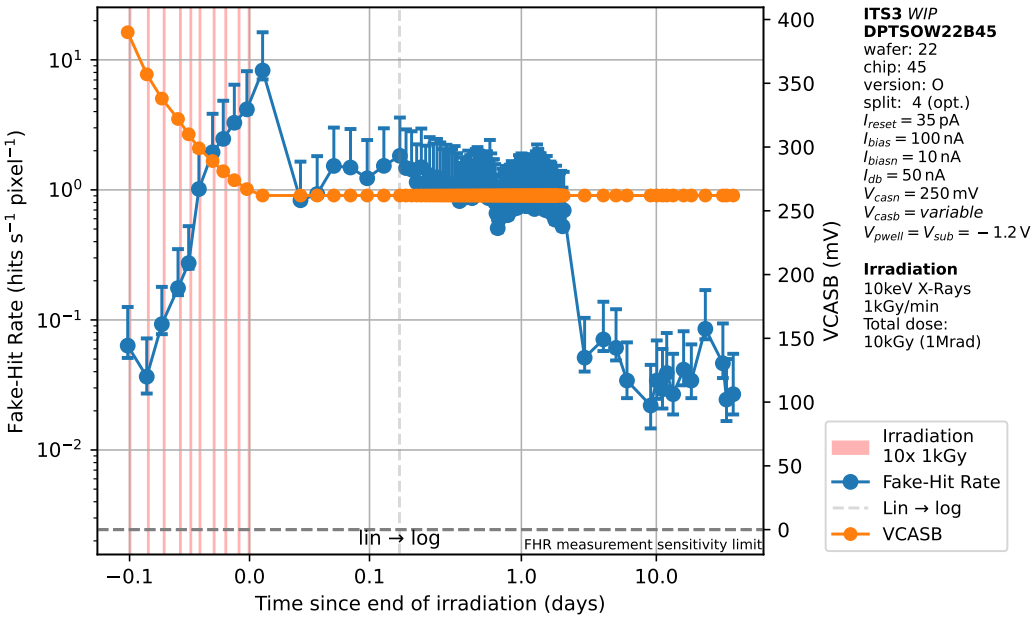


Figure C.14: Fake-hit rate vs. time in a DPTS irradiated up to 10 kGy during and after irradiation. After end of irradiation, the chip was stored at $\approx +20\,^{\circ}C$.

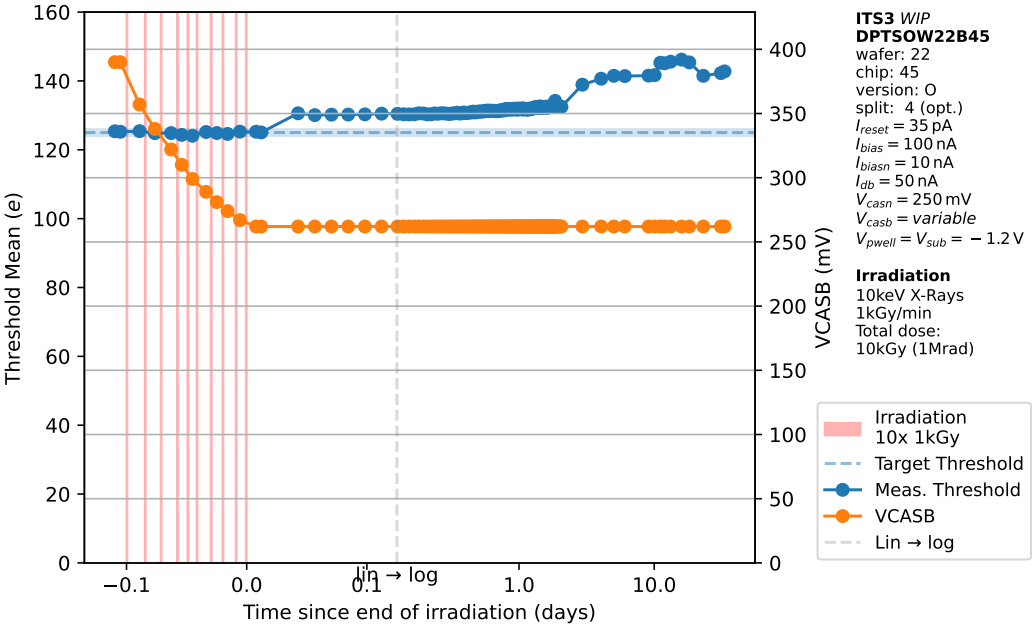


Figure C.15: Threshold mean vs. time in a DPTS irradiated up to 10 kGy during and after irradiation. After end of irradiation, the chip was stored at $\approx +20\,^{\circ}C$.Caption

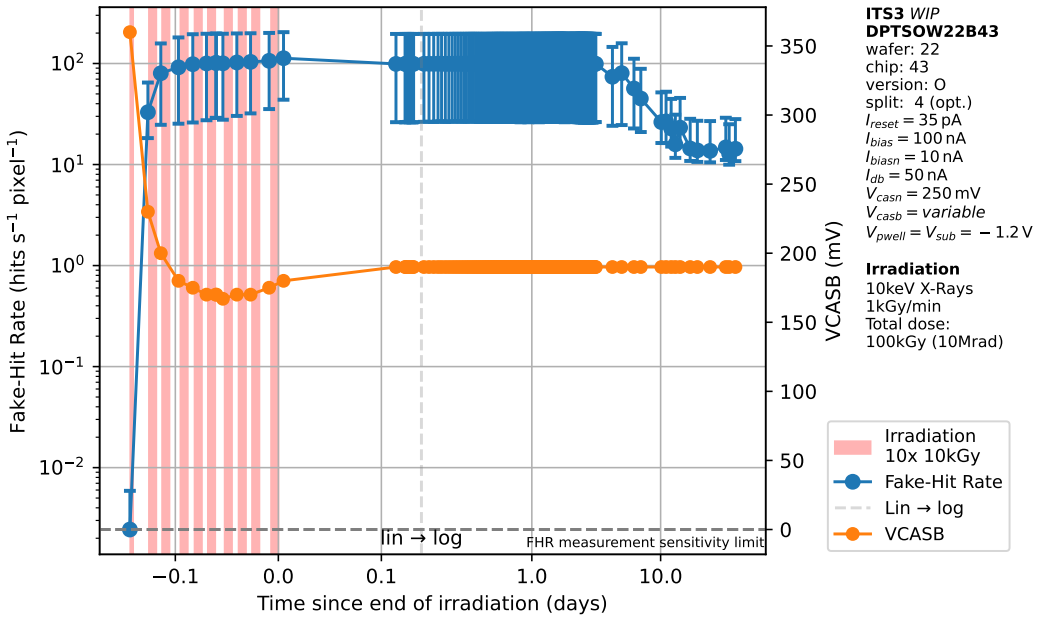


Figure C.16: Fake-hit rate vs. time in a DPTS irradiated up to 100 kGy during and after irradiation. After end of irradiation, the chip was stored at ≈ +20 °C.

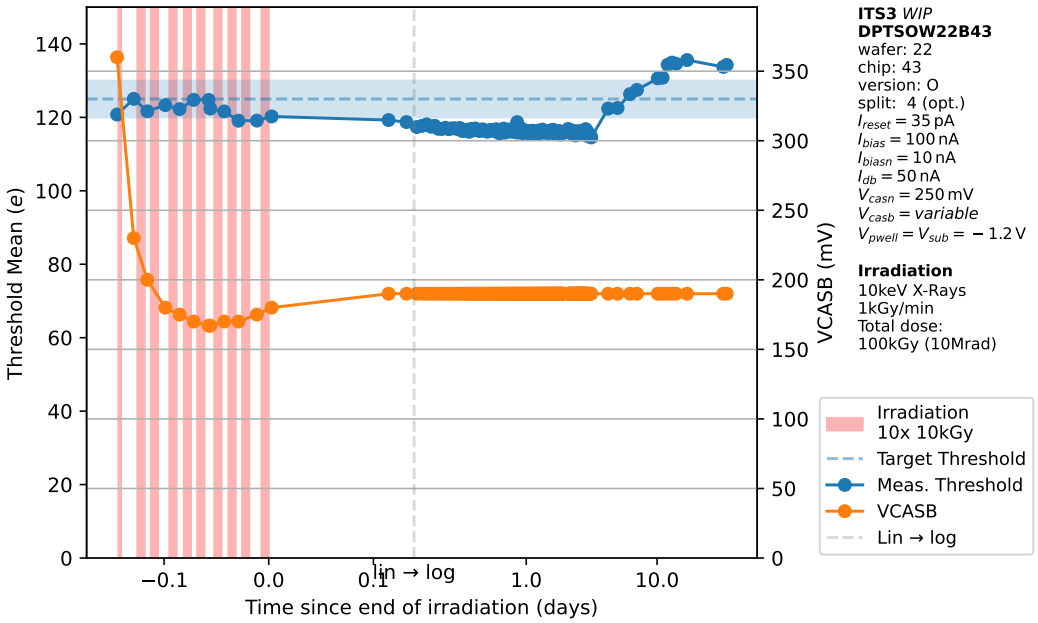


Figure C.17: Threshold mean vs. time in a DPTS irradiated up to 100 kGy during and after irradiation. After end of irradiation, the chip was stored at ≈ +20 °C.

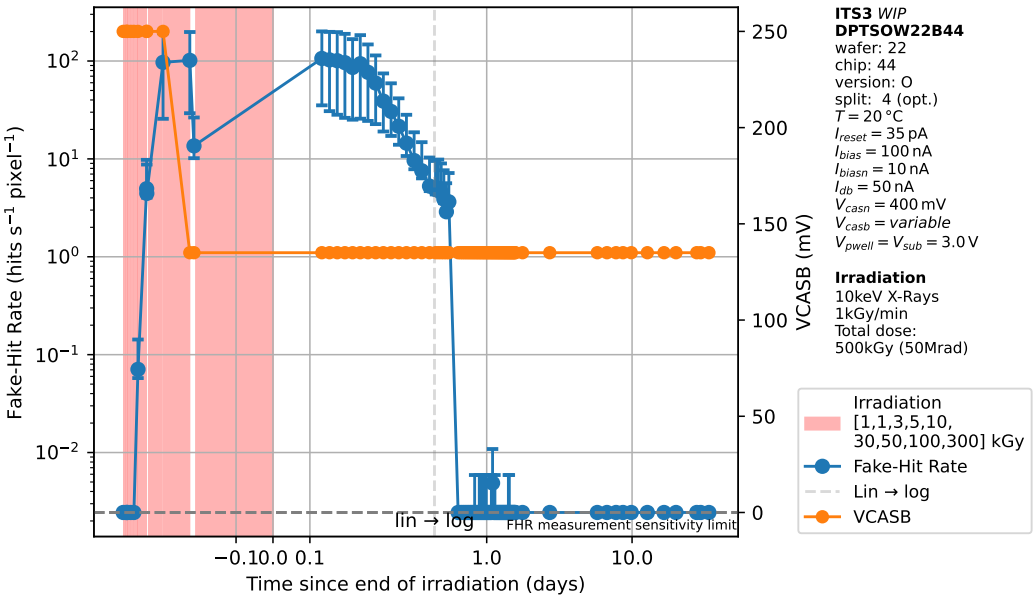


Figure C.18: Fake-hit rate vs. time in a DPTS irradiated up to 500 kGy during and after irradiation. After end of irradiation, the chip was stored at $\approx +20\,°C$.

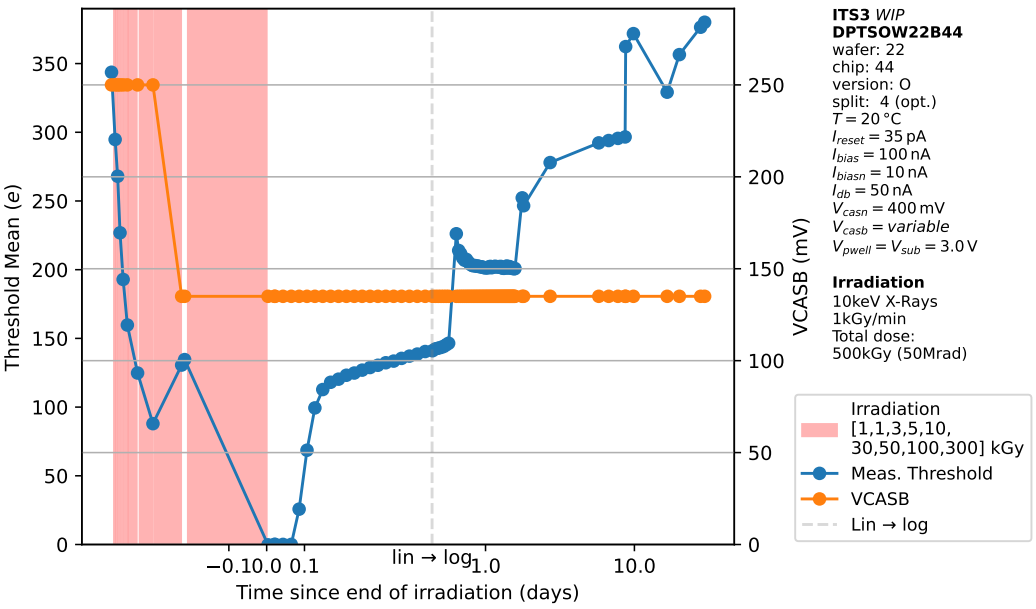


Figure C.19: Threshold mean vs. time in a DPTS irradiated up to 500 kGy during and after irradiation. After end of irradiation, the chip was stored at $\approx +20\,°C$.

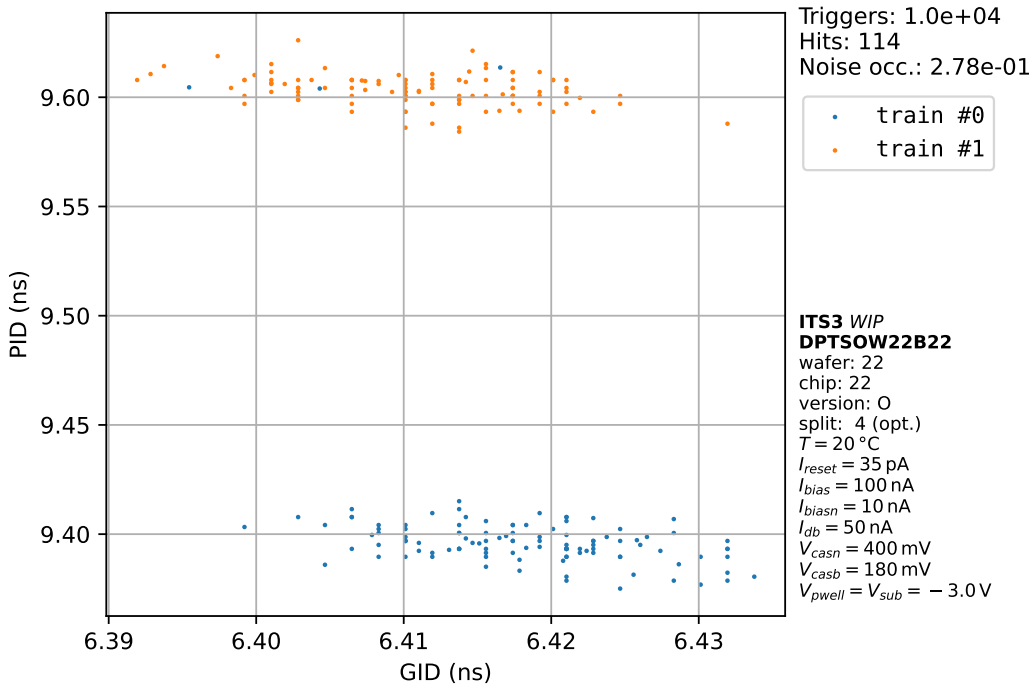


Figure C.20: Result of last fake-hit rate scan of a 5000 kGy sensor taken 67 after the end of the last irradiation step.

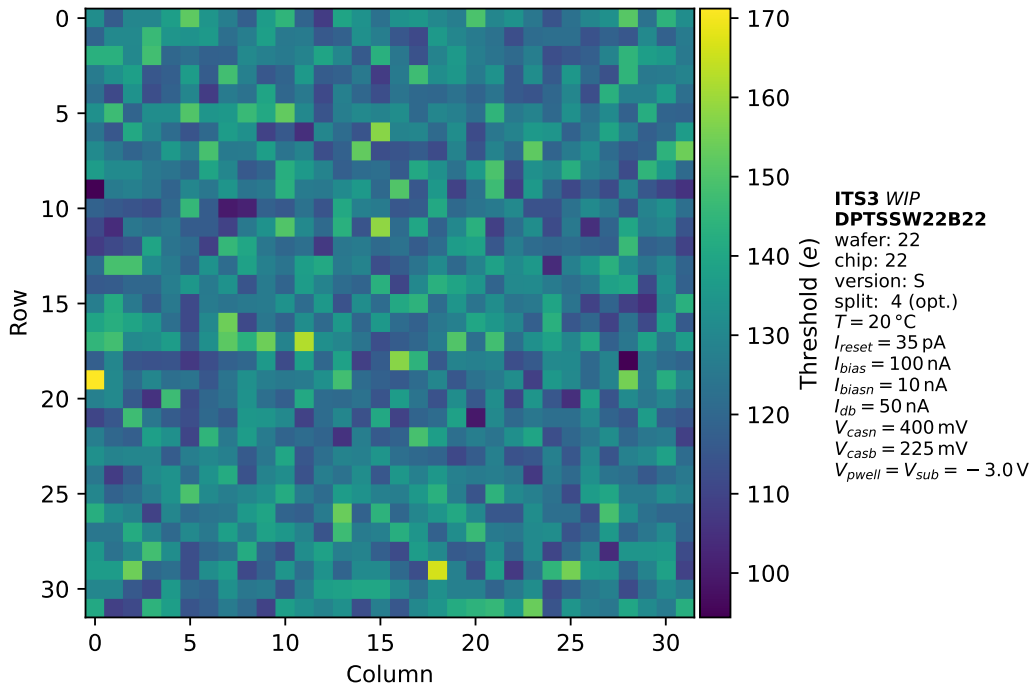


Figure C.21: Threshold map of a 5000 kGy sensor taken 96 after the end of the last irradiation step.

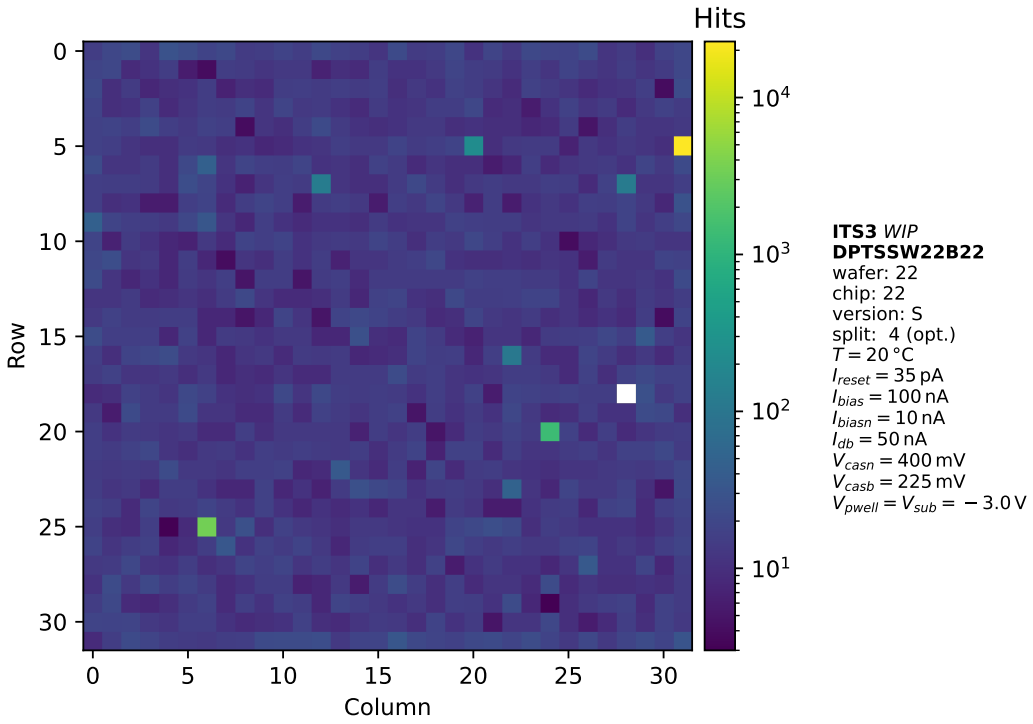


Figure C.22: Hitmap of a 5000 kGy sensor taken 96 after the end of the last irradiation step. Pixel (c=28, r=18) is masked. All other pixel show at least 3 hits.

C.2 Non-Ionizing Radiation

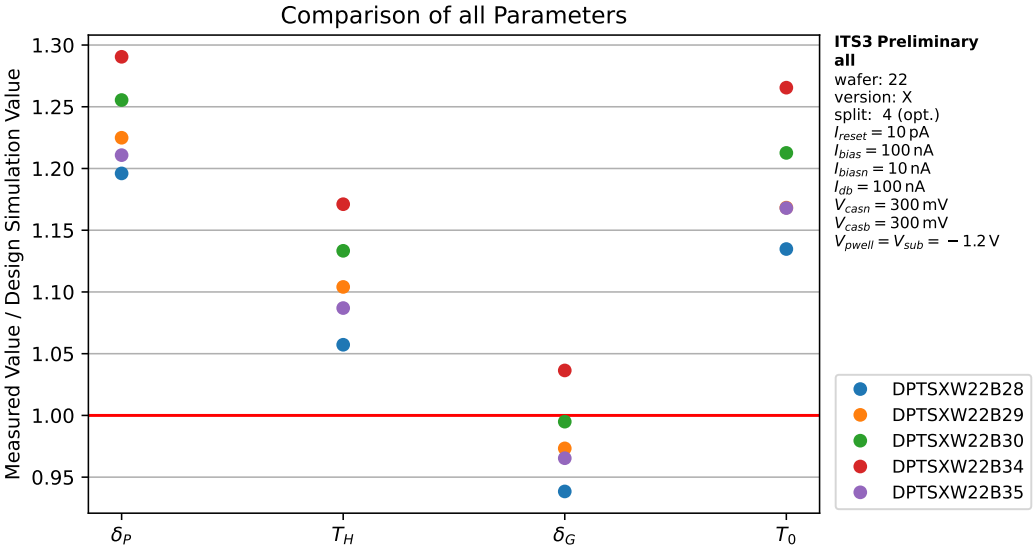


Figure C.23: The four timing of the DPTS (cf. equations (5.1) and (5.2)) for five different non-irradiated chips at same biasing settings.

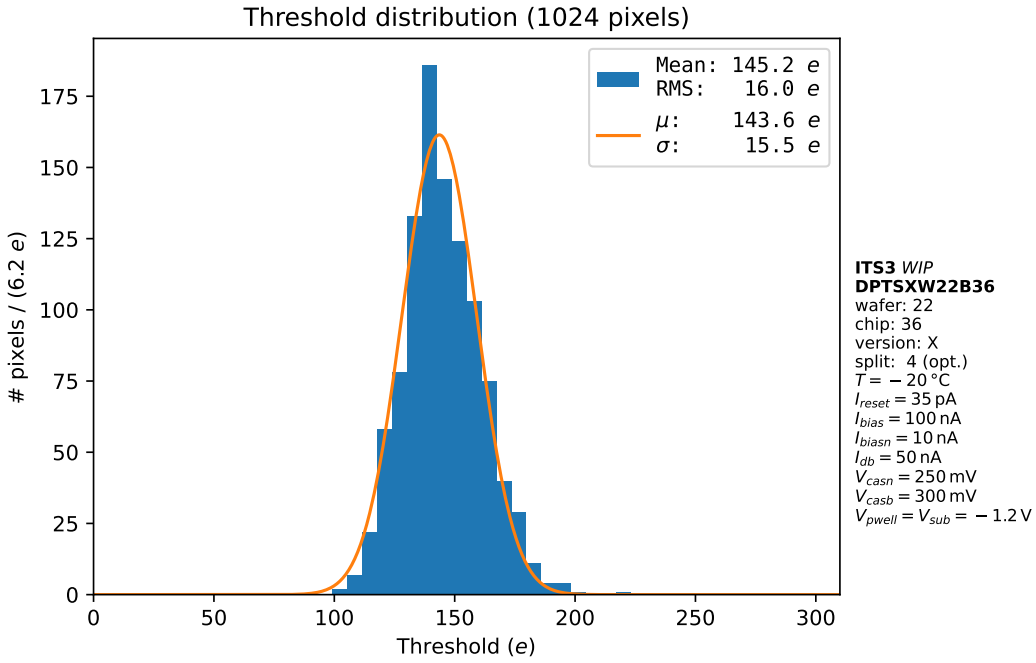


Figure C.24: Threshold scan of a DPTS at $2 \cdot 10^{15}$ 1 MeV n_{eq} cm^{-2} and $-20\,°C$.

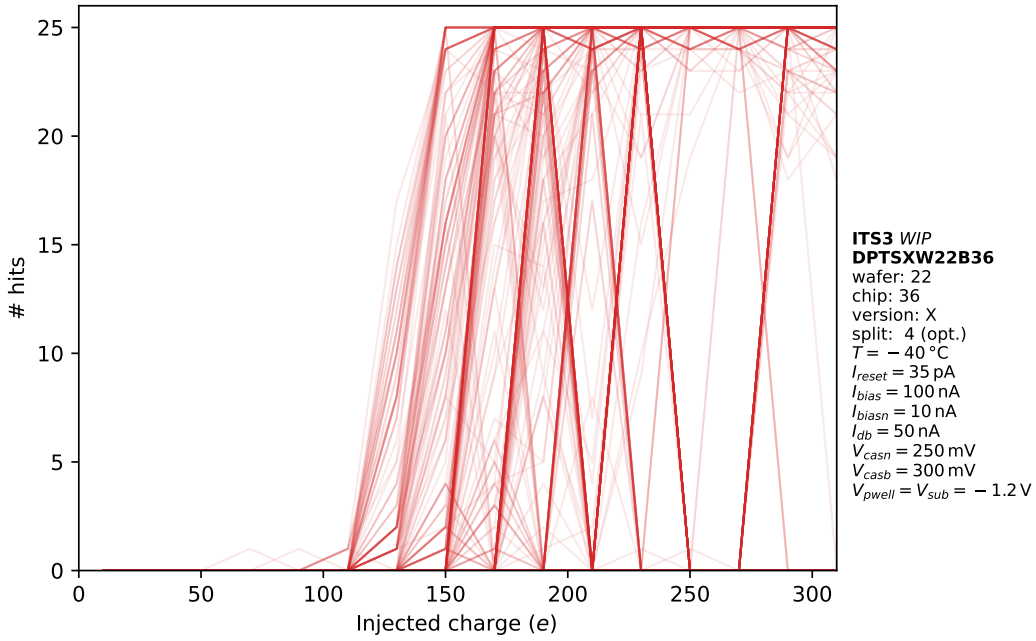


Figure C.25: S-curves of a threshold scan of a DPTS at $2 \cdot 10^{15}$ 1 MeV n_{eq} cm^{-2} and $-40\,°C$.

Bibliography

[Aam+08] K. Aamodt et al. (ALICE collaboration). "The ALICE experiment at the CERN LHC". In: *Journal of Instrumentation* 3.08 (Aug. 2008), S08002–S08002. DOI: 10.1088/1748-0221/3/08/s08002.

[Abe+14] B. Abelev et al. (ALICE collaboration). *Technical Design Report for the Upgrade of the ALICE Inner Tracking System*. Tech. rep. 2014. DOI: 10.1088/0954-3899/41/8/087002.

[Agl+23] G. Aglieri Rinella et al. "Digital pixel test structures implemented in a 65 nm CMOS process". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* (2023), p. 168589. DOI: https://doi.org/10.1016/j.nima.2023.168589.

[Ahl+20] P. Ahlburg et al. "EUDAQ—a data acquisition software framework for common beam telescopes". In: *J. Inst.* 15.01 (Jan. 2020), P01038. DOI: 10.1088/1748-0221/15/01/p01038.

[And+18] A. Andronic et al. "Decoding the phase structure of QCD via particle production at high energy". In: *Nature* 561.7723 (Sept. 2018), pp. 321–330. DOI: 10.1038/s41586-018-0491-6.

[And+83] B. Andersson et al. "Parton fragmentation and string dynamics". In: *Physics Reports* 97.2 (1983), pp. 31–145. DOI: https://doi.org/10.1016/0370-1573(83)90080-7.

[Ber+17] M.J. Berger et al. "Stopping-Power & Range Tables for Electrons, Protons, and Helium Ions". In: *NIST Standard Reference Database* 124 (2017). DOI: 10.18434/T4NC7P.

[Blo06] V. Blobel. "A new fast track-fit algorithm based on broken lines". In: *NIM-A* 566.1 (2006), pp. 14–17. DOI: 10.1016/j.nima.2006.05.156.

[Col22a] ALICE Collaboration. *Letter of intent for ALICE 3: A next-generation heavy-ion experiment at the LHC*. Tech. rep. 2022. arXiv: 2211.02491 [physics.ins-det].

[Col22b] ALICE Collaboration. *The ALICE experiment – A journey through QCD*. 2022. DOI: 10.48550/arXiv.2211.04384. arXiv: 2211.04384 [nucl-ex].

[Dem17] W. Demtröder. *Experimentalphysik 4: Kern-, Teilchen- und Astrophysik*. Springer-Lehrbuch. Springer Berlin Heidelberg, 2017. DOI: 10.1007/978-3-662-52884-6.

[Die+19] R. Diener et al. "The DESY II test beam facility". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 922 (2019), pp. 265–286. DOI: 10.1016/j.nima.2018.11.133.

[DPT21] CERN EP-ESE-ME DPTS Design Team. *Digital Pixel Test Structure Manual*. Not published. Aug. 2021.

[For21] Forthommel. *File:Cern-accelerator-complex.svg*. Last downloaded 09.06.2023. Jan. 2021. URL: https://commons.wikimedia.org/wiki/File:Cern-accelerator-complex.svg.

[Jun08] H. Junde. "Nuclear Data Sheets for A = 55". In: *Nuclear Data Sheets* 109.4 (2008), pp. 787–942. DOI: 10.1016/j.nds.2008.03.001.

[KSW19] J. Kröger, S. Spannagel, and M. Williams. *User Manual for the Corryvreckan Test Beam Data Reconstruction Framework, Version 1.0*. Dec. 2019. arXiv: 1912.00856 [physics.ins-det].

[Mag22] M. Mager. "A truly cylindrical inner tracker for ALICE". In: *PoS* ICHEP2022 (Nov. 2022), p. 318. DOI: 10.22323/1.414.0318.

[Mis19] MissMJ, Cush. *File:Standard Model of Elementary Particles.svg*. Last downloaded 23.08.2023. 2019. URL: https://en.wikipedia.org/wiki/File:Standard_Model_of_Elementary_Particles.svg.

[Mus19] L. Musa. *Letter of Intent for an ALICE ITS Upgrade in LS3*. Geneva, 2019. DOI: 10.17181/CERN-LHCC-2019-018.

[Pir+23] F. Piro et al. "A Compact Front-End Circuit for a Monolithic Sensor in a 65 nm CMOS Imaging Technology". In: *IEEE Transactions on Nuclear Science* (2023), pp. 1–1. DOI: 10.1109/TNS.2023.3299333.

[Pro22] ALICE ITS Project. "First demonstration of in-beam performance of bent Monolithic Active Pixel Sensors". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 1028 (2022), p. 166280. DOI: 10.1016/j.nima.2021.166280.

[Sno+23] W. Snoeys et al. "Optimization of a 65 nm CMOS imaging process for monolithic CMOS sensors for high energy physics". In: *PoS* Pixel2022 (2023), p. 083. DOI: 10.22323/1.420.0083.

[Spi05] H. Spieler. *Semiconductor Detector Systems*. Vol. v.12. Semiconductor Science and Technology. Oxford: Oxford University Press, 2005.

[Tau17] A. Tauro. "ALICE Schematics". General Photo. 2017. URL: http://cds.cern.ch/record/2263642.

[The07] TheNoise. *File:Pn-junction-equilibrium.svg*. Last downloaded 23.08.2023. 2007. URL: https://commons.wikimedia.org/wiki/File:Pn-junction-equilibrium.svg.

[Tho09] Mark Thomson. *Handout 8: Quantum Chromodynamics*. Last downloaded 16.08.2023. 2009. URL: https://www.hep.phy.cam.ac.uk/~thomson/lectures/partIIIparticles/Handout8_2009.pdf.

[Wer+06] N. Wermes et al. *Pixel Detectors, From Fundamentals to Applications*. Springer-Verlag, 2006. DOI: 10.1007/3-540-28333-1.

[Wil14] William M. Haynes. *CRC Handbook of Chemistry and Physics, 95th Edition*. 95th ed. CRC Press, 2014. DOI: 10.1201/b17118.

[Wor+22] R. L. Workman et al. "Review of Particle Physics". In: *PTEP* 2022 (2022), p. 083C01. DOI: 10.1093/ptep/ptac097.

Declaration of Academic Integrity

I, *Nicolas Tiltmann*, hereby confirm that this thesis, entitled "Radiation Hardness of Digital Pixel Sensor Prototypes in 65 nm CMOS Technology for the ALICE ITS3 Upgrade" is solely my own work and that I have used no sources or aids other than the ones stated. All passages in my thesis for which other sources, including electronic media, have been used, be it direct quotes or content references, have been acknowledged as such and the sources cited. I am aware that plagiarism is considered an act of deception which can result in sanction in accordance with the examination regulations.

Münster, 02. September 2023

Nicolas Tiltmann

I consent to having my thesis cross-checked with other texts to identify possible similarities and to having it stored in a database for this purpose.

I confirm that I have not submitted the following thesis in part or whole as an examination paper before.

Münster, 02. September 2023

Nicolas Tiltmann

Acknowledgements

First and foremost, I would like to sincerely thank my group leaders in Münster, Anton Andronic and Christian Klein-Bösing, who gave me the amazing opportunity to spend a year at CERN, where I did the vast majority of work for this master thesis. This has been a truly remarkable experience. Furthermore, I'd like to thank the others of the Münster group who always supported me, even when I was not there.

Moreover, would like to thank my supervisors at CERN, Magnus Mager and Miljenko Šuljić, for their continuous support and all the valuable feedback you gave me. Also, want to thank all other people of the EP-AID-DT group for a wonderful work environment during my year with you.

I sincerely appreciate help with proofreading of my thesis from Matthew Buckland, Francesca Carnesecchi, Hartmut Hillemanns, Ole Kiewe, Marius Menzel, Tim Stellhorn, Peter Stratmann and Anna Villani.

Finally, I am truly thankful to all my friends and last but not least my parents Hildegard and Andreas for their neverending support. Thank you!