# Frequency compensation for fast voltage measurements with the G35 precision HV divider at CRYRING@ESR

#### Master's thesis

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## **Contents**

1	Intr	oductio	on	1
2	Res	earch o	on highly charged ions with CRYRING@ESR	3
	2.1	Resear	rch on highly charged ions	3
	2.2	CRYF	RING as part of the FAIR facility	4
	2.3	Electr	on cooler of CRYRING	5
		2.3.1	Calculation of cooling voltages for different ions	6
	2.4	Dielec	tronic recombination experiments	9
		2.4.1	Electron-ion collision spectroscopy	9
		2.4.2	Variation of collision energies	11
	2.5	Requi	rements for the HV divider	13
3	The	G35 p	recision high voltage divider	15
	3.1	Necess	sity of a high voltage divider	15
	3.2	Electr	ical design of the G35 divider	15
		3.2.1	Primary divider chain	16
		3.2.2	Control divider chain	17
	3.3	Mecha	anical setup of the G35 divider	19
4	Fred	quency	compensation	21
	4.1	Theor	y of frequency compensation	21
	4.2	Freque	ency compensation of a test setup	22
	4.3	Freque	ency compensation of the G35 Divider	28
		4.3.1	LT Spice simulations of the compensated G35 divider	29
		4.3.2	Discussion and consequences of simulation results	33
5	Des	ign of a	a new fast voltage divider	35
	5.1	Electr	ical design and LT-Spice simulations	35
		5.1.1	Calculation of capacitances for compensation	36
		5.1.2	Technical realization	39
		5.1.3	LT spice simulations	40
	5.2	Mecha	unical design	42
		5.2.1	Integrated connections to DVM or oscilloscope	42
6	Con	clusion		45

$C \alpha$		1		1
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References	47
List of Figures	49

## 1 Introduction

Highly charged ions offer a wide range of research opportunities in the fields of nuclear physics, atomic physics, astrophysics and plasma physics. One facility that enables research on highly charged ions is the storage ring CRYRING@ESR<sup>1</sup>. It is part of the new international accelerator center FAIR<sup>2</sup> at the GSI<sup>3</sup> Helmholtzzentrum für Schwerionenforschung in Darmstadt.

An important component of CRYRING is its electron cooler. The process of electron cooling determines the ion energy. Therefore, a precision measurement of the cooler voltage is essential. Since the measurement uncertainty of experiments can be limited by this, measuring the cooler voltage  $\leq 20 \, \text{kV}$  with an accuracy of  $\leq 10 \, \text{ppm}$  is critical<sup>4</sup>. For this purpose, the group of Prof. Weinheimer developed and built the G35 precision high voltage divider at the Institut für Kernyphsik in Münster.

Part of the research program at CRYRING are dielectronic recombination measurements. In these electron-ion collision experiments, the electron cooler of the divider serves both to cool the ions and as an electron target. The collision energies are varied by detuning the electron cooler voltage for short periods of time by applying voltage pulses up to  $\pm 2\,\mathrm{kV}$  lasting 10 ms. For these experiments, the cooler voltage must therefore be measured within 10 ms with the desired accuracy of 10 ppm. The G35 divider was originally designed for static voltage measurements only. Now, the suitability of the G35 divider for fast voltage measurements is under consideration.

The measurement of a sharp high voltage (HV) pulse in a very short time requires a frequency compensation of the HV divider. The aim of this is to adjust all RC elements of the system to the same time constant  $\tau = R \cdot C$  by installing additional capacitors. With perfect compensation, this results in an instantaneous system response for all frequencies. The possibility of a frequency compensation of the G35 divider was first investigated in principle by T. Dirkes in his bachelor thesis [Dir17]. Investigations on the practicability of its implementation are part of this thesis. Due to its limitations, an alternative frequency compensated setup

<sup>&</sup>lt;sup>1</sup>Experimental Storage Ring

<sup>&</sup>lt;sup>2</sup>Facility for Antiproton and Ion Research

<sup>&</sup>lt;sup>3</sup>Gesellschaft für Schwerionenforschung

<sup>&</sup>lt;sup>4</sup> parts per million (10 ppm  $\hat{=}$  10<sup>-5</sup>)

that complements the G35 divider is proposed.

The structure of this thesis is as follows. Chapter 2 gives a short overview of research on highly charged ions and introduces FAIR/GSI and CRYRING@ESR in particular. The electron cooler and the dielectronic recombination experiments are described with regard to the requirements for high voltage measurements.

Chapter 3 deals with the G35 precision high voltage divider. The principle of operation and its electrical and mechanical design are explained.

Chapter 4 covers the frequency compensation of voltage dividers. The principle of frequency compensation is demonstrated by measurements on a compensated test setup. A possible frequency compensation of the G35 divider with its limitations is investigated by performing simulated transient analyses of the system.

In Chapter 5, an alternative realization in form of a separate frequency compensated high voltage divider complementing the G35 divider is proposed. The electrical design and its possible technical implementation are illustrated.

Chapter 6 summarizes the results and gives an outlook on future proceedings.

# 2 Research on highly charged ions with CRYRING@ESR

This chapter gives an overview of research on highly charged ions. The storage ring CRYRING@ESR is introduced next. Its electron cooler and the dielectronic recombination experiments are described with regard to the requirements for high voltage measurements.

## 2.1 Research on highly charged ions

Highly charged ions (HCI) provide the highest (local) electric and magnetic fields accessible in laboratories. The blue curve in figure 2.1 shows the electric field strength present at the 1s shell electrons of highly charged ions in relation to the nuclear charge Z of the ion. For high Z, field strengths  $> 10^{15} \,\mathrm{V/cm}$  occur, three orders of magnitude higher than the field strength achievable with the 300 TW Hercules laser at University of Michigan, one of the most powerful lasers in the world. HCI are therefore used for tests of atomic properties under extreme conditions, such as relativistic and electron-correlation effects as well as the validity of QED calculations in extremely high field strengths. Experimental approaches

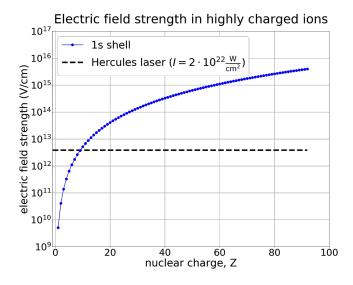
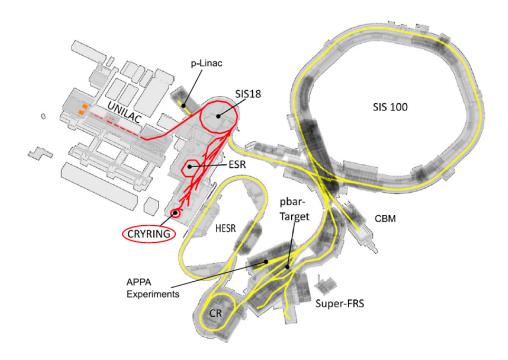


Figure 2.1: Electric field strength in highly charged ions compared to the Hercules laser [Win18a].



**Figure 2.2:** Layout of new FAIR facilities and existing GSI facilities and the position of CRYRING [Gei17].

to study HCI include among others laser spectroscopy and electron-ion collision spectroscopy. CRYRING@ESR is a storage ring used for HCI research and will be described in the next section.

## 2.2 CRYRING as part of the FAIR facility

CRYRING@ESR is a heavy ion storage ring that is part of the new international accelerator facility FAIR at GSI Helmholtzzentrum für Schwerionenforschung in Darmstadt. The existing accelerator facilities at GSI will serve as the injector for FAIR. The position of CRYRING and a layout of the FAIR facilities are shown in figure 2.2. CRYRING was originally built by the Manne Siegbahn Laboratory (MSL) in Stockholm and served more than twenty years successfully to their research in atomic and molecular physics. As the Swedish in-kind contribution to FAIR, it was transferred to GSI in the years 2012 and 2013. After reconstruction and modernization, it was put into operation in 2017. It will be used for research with slow exotic ion beams by FAIR collaborations like SPARC<sup>1</sup>, FLAIR<sup>2</sup> and NuSTAR<sup>3</sup> as well as for testing new FAIR slow control technologies.

<sup>&</sup>lt;sup>1</sup>Support Program for Advancing Research and Collaboration

<sup>&</sup>lt;sup>2</sup>Facility for Low-energy Antiproton and Ion Research

<sup>&</sup>lt;sup>3</sup>Nuclear Structure, Astrophysics and Reactions

Figure 2.3 shows the CRYRING setup in more detail. It is set up downstream of the Experimental Storage Ring (ESR) and can decelerate, store and cool ions with a maximum energy of  $30\,\mathrm{MeV/nucleon}$  down to a few  $100\,\mathrm{keV/nucleon}$ . A standalone operation independent of FAIR accelerators is possible with a local ion source providing low energy ions up to  $E \leq 300\,\mathrm{keV/u}$ . CRYRING has a circumference of  $54\,\mathrm{m}$ . Twelve  $30^\circ$  magnetic dipoles and a number of magnetic quadrupoles and sextupoles keep the ions in orbit. Further sections contain an injection, an extraction system and an RF cavity for deceleration and acceleration. One section is used for experiments, e.g. a gas target, and one contains the electron cooler to provide a better beam quality by phase-space cooling. The electron cooler is described in more detail in the next section.

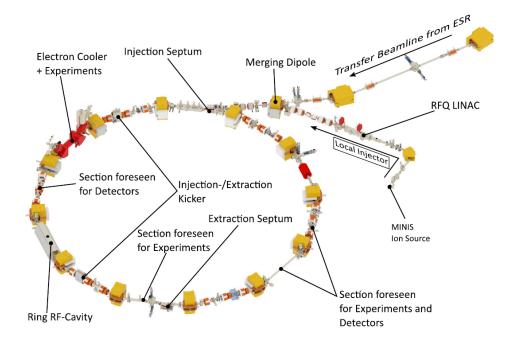


Figure 2.3: Overview of the CRYRING@ESR setup [Gei17].

#### 2.3 Electron cooler of CRYRING

The electron cooler of CRYRING works by aligning the ion beam collinearly with a mono-energetic electron beam with a velocity close to the average ion velocity. Figure 2.4 shows a schematic of the setup and its components. The electrons are produced by an electron gun which is surrounded by a superconducting solenoid magnet and cooled via a cryo-system using liquid helium. Usually, electron currents during operation are in the order of 100 mA [Dan11]. Bent magnets guide the electrons on to the ion beam path and off of it at the end of the electron cooler. This cooling section has a length of 1.1 m.

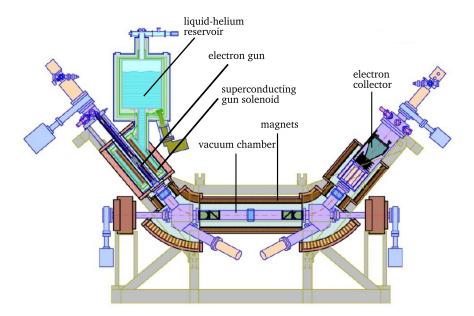


Figure 2.4: Schematic of the electron cooler of CRYRING [Dan11].

Coulomb scattering during the collinear alignment of electron and ion beam leads to an energy exchange until the thermodynamic equilibrium is reached where electrons and ions have the same velocity. The ion velocity is therefore dependent on the energy of the electrons. Precision measurements of the electron energy are essential to improve the knowledge of the ion velocity. The electron energy is determined by the acceleration voltage  $U_{\rm cool} \leq 20\,\rm kV$ . High voltage measurements with a precision voltage divider designed for that purpose are described in section 3.1. The electron cooler also serves as target for a merged-beams electron-ion collision spectroscopy setup which will be presented in section 2.4.

#### 2.3.1 Calculation of cooling voltages for different ions

In this section, the magnitude of the necessary cooling voltage for different ions is calculated. During the cooling process, the velocities of ions and electrons are the same. In the relativistic case, their Lorentz factors are then identical:  $\gamma_i \equiv \gamma_e$ . The kinetic electron energy in the cooling section is  $^4$   $E_{\rm e,kin} = e \cdot U_{\rm cool}$ , so that follows:

$$\gamma_{\rm e} = 1 + \frac{E_{\rm e,kin}}{m_{\rm e}c^2} = 1 + \frac{E_{\rm i,kin}}{m_{\rm i}c^2} = \gamma_{\rm i} \Leftrightarrow$$

$$E_{\rm i,kin} \frac{m_{\rm e}}{m_{\rm i}} = E_{\rm e,kin} = e \cdot U_{\rm cool}$$
(2.1)

where  $m_{\rm e}$  is the electron rest mass,  $m_{\rm i}$  is the ion mass and c is the speed of light. The maximum cooling voltage therefore depends on the maximum achievable

<sup>&</sup>lt;sup>4</sup>neglecting the space charge potential  $U_{\rm sc} \ll U_{\rm cool}$ .

kinetic energy of the ions. In a storage ring,  $E_{i,kin}$  is limited by the magnetic rigidity  $B\rho$  of the device. An ion moving in the ring is held on track by the balance of centripetal force and Lorentz force:

$$\frac{\gamma_i m_i v_i^2}{\rho} = Q_i v_i B, \tag{2.2}$$

with Lorentz factor  $\gamma_i$ , mass  $m_i$ , velocity  $v_i$  and charge  $Q_i$  of the ion, the magnetic field B and the radius  $\rho$  of the ring. For the maximum momentum  $p_{\text{max}}$  follows:

$$p_{\text{max}} = \gamma_{\text{i}} m_{\text{i}} v_{\text{i}} = Q_{\text{i}} (B\rho)_{\text{max}}. \tag{2.3}$$

The CRYRING has a rigidity of  $(B\rho)_{\text{max}} = 0.8 \,\text{T}$  m for protons/anti-protons and  $(B\rho)_{\text{max}} = 1.44 \,\text{T}$  m for other ions [Les16]. For the maximum kinetic energy of the ions follows:

$$E_{i,kin}^{max} = E_{i,tot} - m_i c^2 = \sqrt{p_{max}^2 c^2 + m_i^2 c^4} - m_i c^2.$$
 (2.4)

**Proton** A proton with mass<sup>5</sup>  $m_p = 938.272 \,\text{MeV}/c^2$ , charge Q = 1e and  $p_{\text{max}} = e \cdot 0.8 \,\text{T}$  m has the following maximum kinetic energy in the CRYRING:

$$E_{\rm p,kin}^{\rm max} = \sqrt{(e \cdot 0.8 \, {\rm T\, m})^2 c^2 + (938.272 \, {\rm MeV})^2} - 938.272 \, {\rm MeV} = 30.17 \, {\rm MeV}$$

With equation 2.1 and the electron mass  $m_e = 511 \text{ keV}/c^2$ , the necessary cooling voltage  $U_{\text{cool}}$  becomes:

$$U_{\text{cool}} = \frac{30.17 \,\text{MeV}}{e} \cdot \frac{511 \,\text{keV}}{938.272 \,\text{MeV}} = 16.4 \,\text{kV}$$

**Light ion** Other ions have the mass number M = n(protons) + n(neutrons) and the charge  $Q = Z \cdot e$  with the atomic number Z. For these<sup>6</sup>  $Z/M \leq 0.5$  holds. Applying equation 2.3 for a light ion with Z/M = 0.5 yields:

$$p_{\text{i.max}} = Z \cdot e(B\rho)_{\text{max}} = 0.5 \cdot M \cdot e \cdot 1.44 \,\text{T m} = M \cdot e \cdot 0.72 \,\text{T m}$$

The ion mass  $m_i$  can be expressed as:

$$m_{\rm i} = M \cdot \tilde{m}_N \quad \text{with} \quad \tilde{m}_N = 930.5 \,\text{MeV}/c^2,$$
 (2.5)

<sup>&</sup>lt;sup>5</sup>This value and other constants are taken from [NIST]

<sup>&</sup>lt;sup>6</sup>except <sup>3</sup>He

where  $\tilde{m}_N$  is an estimate of the mean nucleon mass minus the binding energy per nucleon. Using equation 2.4, the maximum kinetic energy for this ion is:

$$E_{i,kin}^{max} = M\left(\sqrt{(e \cdot 0.72 \,\mathrm{T\,m})^2 c^2 + \tilde{m}_N^2 c^4} - \tilde{m}_N c^2\right) = M \cdot 24.71 \,\mathrm{MeV}^7$$

With equation 2.1 follows for the cooling voltage:

$$U_{\text{cool}} = \frac{M \cdot 24.71 \,\text{MeV}}{e} \cdot \frac{511 \,\text{keV}}{M \cdot 930.5 \,\text{MeV}} = 13.6 \,\text{kV}.$$

**Heavy ion** An example for a heavy highly charged ion is lithium-like uranium  $^{238}\mathrm{U}^{89+}$  with  $Z/M=89/238\approx0.374$ . With equation 2.3 follows:

$$p_{i,\text{max}} = Z \cdot e(B\rho)_{\text{max}} = M \cdot e \cdot 0.538 \,\text{T m}.$$

The mass of  $^{238}\mathrm{U}^0$  is  $238.05\,\mathrm{u}$ . The ion mass of  $^{238}\mathrm{U}^{89+}$  is estimated as:

$$m_{\rm i} \approx 238.00 \,\mathrm{u} = M \cdot \mathrm{u} \quad \text{with} \quad 1 \,\mathrm{u} = 931.494 \,\mathrm{MeV}/c^2.$$
 (2.6)

The maximum kinetic energy of the heavy ion is therefore:

$$E_{i,kin}^{\max} = M\left(\sqrt{(e \cdot 0.538 \,\mathrm{T\,m})^2 c^2 + (931.494 \,\mathrm{MeV})^2} - 931.494 \,\mathrm{MeV}\right) = M \cdot 13.89 \,\mathrm{MeV}.$$

And the corresponding cooling voltage is:

$$U_{\rm cool} = \frac{M \cdot 13.89 \, \text{MeV}}{e} \cdot \frac{511 \, \text{keV}}{M \cdot 931.494 \, \text{MeV}} = 7.6 \, \text{kV}.$$

In conclusion, cooling voltages up to 16.4 kV are needed in principle, while voltages of about 8 kV are sufficient for heavy ion experiments.





**Figure 2.5:** Photos of the CRYRING setup (left) and a close up of the electron cooler (right) [Hos17].

<sup>&</sup>lt;sup>7</sup>In the literature the kinetic energy of ions is sometimes given in the unit MeV/u which is technically incorrect because the unified atomic mass unit u has the dimension [kg]

## 2.4 Dielectronic recombination experiments

Electron-ion collisions offer various ways for research on the atomic structure of HCI. By studying elastic scattering, ionization, excitation or recombination, modern atomic theory can be tested with respect to the validity of QED as well as relativistic and nuclear effects [Les16]. They are also most relevant in astrophysics and plasma physics where they determine the emitted electromagnetic spectrum, e.g. in X-ray studies [Mül08]. Relevant for this thesis are precision electron spectroscopy experiments via dielectronic recombination (DR) at low energies because the energy resolution is highest there due to the kinematics of the merged-beams setup. The principle and methods of the experiments are presented in the next sections.

Examples for DR experiments at ion storage rings include measurements of isotope shifts with  $Pb^{53+}$  at CRYRING located at the MSL in Stockholm [Sch05] or with  $Nd^{57+}$  at the ESR in Darmstadt [Bra08] as well as measurements of hyperfine-split dielectronic resonances in lithium-like  $Sc^{18+}$  at the test storage ring TSR in Heidelberg [Les08].

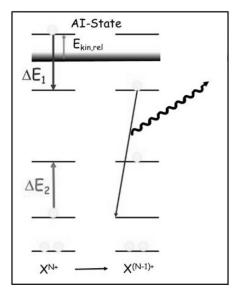


Figure 2.6: Principle of dielectronic recombination [Les14].

#### 2.4.1 Electron-ion collision spectroscopy

Merged-beams setups performing electron-ion collision spectroscopy usually focus on the atomic process of DR. The principle of DR is shown in figure 2.6. It can be seen as a two step process. In the first step, called dielectronic capture, a free electron from an external target falls into a doubly-excited resonance state of an ion with charge N. The energy gain  $\Delta E_1$  has to match the energy difference  $\Delta E_2$ 

required for the excitation of a bound electron to a doubly-excited state. Hence, dielectronic capture is a resonant process which can be seen as time-reversed autoionization. In the second recombination step, the ion with charge N-1 de-excites by emission of photons

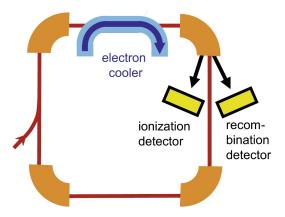
$$X^{N+} + e^- \to X^{(N-1)+**} \to X^{(N-1)+*} + \text{photon(s)}.$$
 (2.7)

A competing process to DR is the so called radiative recombination (RR) where the electron falls into a bound subshell of the ion with emission of a photon.

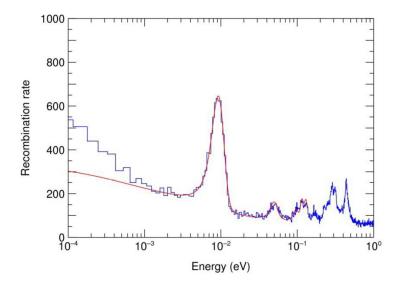
$$e + X^{N+} \to X^{(N-1)+} + h\nu$$
 (2.8)

While DR produces resonance peaks, RR is responsible for a continuous background in the recombination spectrum. Figure 2.7 shows a sketch of an electronion collision spectroscopy setup. After collision in the electron cooler, the new ions are separated via their charge and collected in the detectors. The position of the detectors depends on the studied process and the new charge of the collected particles.

Figure 2.8 is an example of a low energy DR spectrum measured at the CRYRING electron cooler in Stockholm. It shows the rate of collected ions  $X^{(N-1)+*}$  vs. the relative collision energy between ions and electrons. One sees the DR resonance peaks on top of the RR background. The scanning of the relative collision energies is explained in the next section.



**Figure 2.7:** Schematic of an electron-ion collision spectroscopy experiment setup at a storage ring [Sch14].



**Figure 2.8:** Low-energy DR resonances of F<sup>6+</sup> as measured at the CRYRING electron cooler in Stockholm. The red curve is a fit to the blue experimental spectrum [BLS14].

#### 2.4.2 Variation of collision energies

In the collision experiment, the electron beam functions as cooling for the ions as well as the electron target. Therefore a special scanning procedure has to be applied. The collision energies are finely scanned by repeated swift and precise detuning of the electron cooler voltage. The ion beam is cooled by electrons with a base potential  $U_{\text{cool}}$ . The electron energy in the laboratory  $E_{\text{e,kin}}$  is varied by an additional detuning voltage  $U_{\text{det}}$  on top of  $U_{\text{cool}}$ . Besides the applied voltages, also the space-charge potential  $U_{\text{sc}}$  of the electrons has to be taken into account. Without detuning,  $U_{\text{det}} = 0$ , ions and electrons have the same velocity due to the cooling process. Hence, the relativistic Lorentz factor of ions (i) and electrons (e) is the same  $\gamma_{\text{i}} \equiv \gamma_{\text{e}}$ . Detuning changes  $\gamma_{\text{e}}$  in the following way:

$$\gamma_{\rm e} = \frac{E_{\rm e,tot}}{m_{\rm e}c^2} = 1 + \frac{E_{\rm e,kin}}{m_{\rm e}c^2} = 1 + \frac{e(U_{\rm cool} + U_{\rm det} + U_{\rm sc})}{m_{\rm e}c^2},$$
(2.9)

where  $m_e$  is the electron rest mass and c is the speed of light. While  $\gamma_i$  stays constant for a short period of time, the change of  $\gamma_e$  introduces a relative collision energy. The energy in the center-of-mass (CM) frame  $E_{\rm CM}$  can be calculated by analysing the invariant Mandelstam variable  $s = (p_i + p_e)^2$  of the 4-momentum vectors  $p_i$  and  $p_e$  with

$$p_{i} + p_{e} = \begin{pmatrix} \frac{E_{i,tot}}{c} \\ \underline{p_{i}} \end{pmatrix} + \begin{pmatrix} \frac{E_{e,tot}}{c} \\ \underline{p_{e}} \end{pmatrix} = \begin{pmatrix} \frac{E_{i,tot} + E_{e,tot}}{c} \\ \underline{p_{i}} + \underline{p_{e}} \end{pmatrix}, \tag{2.10}$$

so that  $E_{\rm CM}/c = \sqrt{s}$  is

$$E_{\rm CM} = \left[ (E_{\rm i,tot} + E_{\rm e,tot})^2 - \left( \underline{p}_{\rm i} + \underline{p}_{\rm e} \right)^2 c^2 \right]^{\frac{1}{2}}.$$
 (2.11)

Using  $E_{\text{tot}} = E_{\text{kin}} + mc^2$  and  $E_{\text{tot}}^2 = p^2c^2 + m^2c^4$  yields:

$$\begin{split} E_{\mathrm{CM}} &= \left[ \underline{p}_{\mathrm{i}}^2 c^2 + m_{\mathrm{i}}^2 c^4 + \underline{p}_{\mathrm{e}}^2 c^2 + m_{\mathrm{e}}^2 c^4 + 2 \left( E_{\mathrm{i},\mathrm{kin}} + m_{\mathrm{i}} c^2 \right) \left( E_{\mathrm{e},\mathrm{kin}} + m_{\mathrm{e}} c^2 \right) \right. \\ &\left. - \left( \underline{p}_{\mathrm{i}}^2 c^2 + \underline{p}_{\mathrm{e}}^2 c^2 + 2 |\underline{p}_{\mathrm{i}}| \cdot |\underline{p}_{\mathrm{e}}| \cos(\theta) c^2 \right) \right]^{\frac{1}{2}}, \end{split}$$

where  $\theta$  is the laboratory angle between ion beam and electron beam. With  $|\underline{p}| = \sqrt{E_{\rm kin}(E_{\rm kin} + 2mc^2)}/c$  follows:

$$E_{\rm CM} = \left[ \left( m_{\rm i} c^2 + m_{\rm e} c^2 \right)^2 + 2 \left( E_{\rm i,kin} E_{\rm e,kin} + E_{\rm i,kin} m_{\rm e} c^2 + E_{\rm e,kin} m_{\rm i} c^2 \right. - \sqrt{E_{\rm i,kin} (E_{\rm i,kin} + 2m_{\rm i} c^2)} \sqrt{E_{\rm e,kin} (E_{\rm e,kin} + 2m_{\rm e} c^2)} \cos(\theta) \right]^{\frac{1}{2}}.$$
 (2.12)

For the collision energy  $E_{\rm col}$ , one has to subtract the rest masses:

$$E_{\rm col} = E_{\rm CM} - m_{\rm i}c^2 - m_{\rm e}c^2. \tag{2.13}$$

With equations 2.9, 2.12, and 2.13,  $E_{\text{col}}$  can be calculated in dependence of  $U_{\text{det}}$ . Figure 2.9 shows a plot of this for typical ion energies of CRYRING. Examples of  $U_{\text{det}}$  for specific values of  $E_{\text{col}}$  are shown in table 2.1 for a heavy ion beam

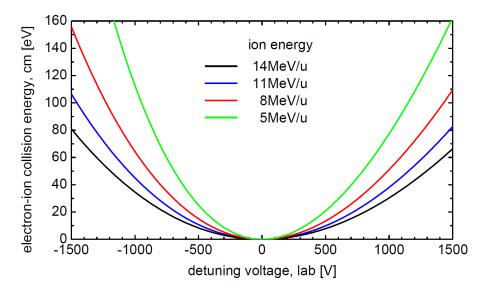


Figure 2.9: Relative collision energy  $E_{\rm col}$  in the CM frame in dependence of the detuning voltage  $U_{\rm det}$  in the laboratory for typical ion energies of CRYRING [BLS14].

$E_{\rm col}$	$U_{ m det}$	
$1\mathrm{eV}$	$\approx 175\mathrm{V}$	
$10\mathrm{eV}$	$\approx 545\mathrm{V}$	
$100\mathrm{eV}$	$\approx 1660\mathrm{V}$	

**Table 2.1:** Detuning voltages  $U_{\text{det}}$  for specific values of  $E_{\text{col}}$  for an ion beam with an energy of  $E_{\text{i,kin}} = M \cdot 14 \,\text{MeV}$  [BLS14].

with an energy of  $E_{\rm i,kin} = M \cdot 14\,{\rm MeV}$ . As shown in section 2.3.1, this is the maximum achievable energy which ensures the longest beam lifetime as well as a reduction of background by collisions with the residual gas. For the detuning voltage, a fast HV amplifier with  $\pm 2\,{\rm kV}$  will be used. The scanning procedure of alternating detuning and cooling steps in the order of 10 ms is shown in figure 2.10. Intermittent cooling steps with  $U_{\rm cool}$  are necessary to maintain the ion energy and beam quality. The detuning voltages are calculated for a linear change of  $E_{\rm col}$  in each step [BLS14].

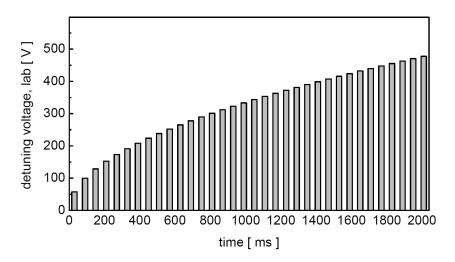


Figure 2.10: Procedure for energy scanning with detuning voltages and intermediate cooling [BLS14].

## 2.5 Requirements for the HV divider

As described earlier, the HV measurements for the electron cooler at CRYRING have to achieve two different goals. The first goal is to measure the static cooling voltage  $U_{\text{cool}}$ . Laser spectroscopy experiments of hyperfine transitions at the ESR were initially limited due to the measurement accuracy of the electron cooler voltage. The accuracy of the transition energies could be improved by using a pre-

cision high voltage divider of the Physikalisch-Technische Bundesanstalt<sup>8</sup> [Vol15]. Therefore CRYRING has its own voltage divider to measure the electron cooler voltage with an uncertainty below 10 ppm. For this purpose, the group of Prof. Weinheimer developed and built the G35 precision high voltage divider at the Institut für Kernyphsik in Münster.

The second goal is to measure the electron cooler voltages with an uncertainty in the 10 ppm range during dielectronic recombination experiments in a time frame of 10 ms. The G35 divider was originally designed for the static DC measurements. It can in principle also be used for measurements faster than 10 ms by installing a frequency compensation which was investigated by T. Dirkes in his bachelor thesis [Dir17]. Further investigations on the practicability and realization of the frequency compensation will be part of this thesis.

<sup>&</sup>lt;sup>8</sup>National Metrology Institute of Germany

## 3 The G35 precision high voltage divider

As described in chapter 2, precision high voltage measurements are required for experiments at CRYRING@ESR. The G35 precision high voltage divider developed for that purpose will be presented in this chapter.

## 3.1 Necessity of a high voltage divider

A measurement of the electron cooler voltage with an accuracy below 10 ppm is required to reduce the measurement uncertainty of the ion velocities as described in section 2.3. Commercially available 8.5-digit digital voltmeters (DVM) are most precise in their ~10 V range. Therefore, the electron cooler voltage  $U_{\rm cool} \leq 20 \, \rm kV$  cannot be measured directly and will be applied to a voltage divider first with the purpose of scaling down  $U_{\rm cool}$  to a voltage in the most precise range of a DVM. The precision and stability of the divider must ensure that  $\Delta U_{\rm cool}/U_{\rm cool} < 10^{-5}$ . The design of the G35 HV divider is based on the two custom made ultra-precise KATRIN<sup>1</sup> HV dividers which were developed at the Institut für Kernyphsikin Münster in cooperation with the Physikalisch-Technische Bundesanstalt<sup>2</sup> [Thü09, Bau13].

For a more flexible use, e.g. low energy operations of the ESR, the G35 divider is designed for input voltages up to 35 kV.

## 3.2 Electrical design of the G35 divider

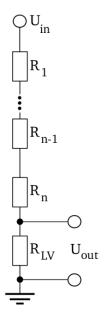
The principle of an electric circuit for a voltage divider is shown in figure 3.1. The higher input voltage  $U_{\rm in}$  is applied to a chain of resistors. For a purely ohmic voltage divider, the resistors form ohmic resistances  $R_1, ..., R_n, R_{\rm LV}$  in series. The lower output voltage  $U_{\rm out}$  is measured across  $R_{\rm LV}$ . It is scaled down depending on the ratio of resistances which is defined as the scale factor M:

$$M = \frac{U_{\rm in}}{U_{\rm out}} = \frac{\sum_{i=1}^{n} R_i + R_{\rm LV}}{R_{\rm LV}}.$$
 (3.1)

The G35 divider consists of two divider chains. One is the primary divider chain

<sup>&</sup>lt;sup>1</sup>KArlsruhe TRItium Neutrino experiment

<sup>&</sup>lt;sup>2</sup>National Metrology Institute of Germany



**Figure 3.1:** Electric circuit diagram for an ohmic voltage divider.

for precision high voltage measurements as described above. The other is the so called control divider chain which is laid out as a mixed ohmic/capacitive divider. Both chains are described in more detail in the following sections.

Figure 3.2 shows the equivalent circuit of the electrical design of the G35 divider with the respective values of the used components. On the left hand side one sees the control divider chain which has protective and stabilizing functions as well as the primary divider chain of resistances  $R_1$  to  $R_{65}$  and  $R_{LV}$ . The control divider chain is made up of resistances  $R_{CD}$  and  $R_{CD, LV}$  as well as capacitances  $C_{CD}$  and  $C_{CD, LV}$ . The right hand side shows in detail how the low voltage part  $R_{LV}$  is realized to achieve five different scale factors M. In total, it consists of 16 resistors with resistances  $R_{LV,1}$ ,  $R_{LV,2}$  and  $R_{LV,3}$ .

#### 3.2.1 Primary divider chain

As indicated in figure 3.2, the voltage divider is composed of 5 sections. For the primary divider chain, the top 4 sections include the 65 precision high voltage resistors of type VISHAY VHA518-11 with  $1.84\,\mathrm{M}\Omega$ . These bulk-metal foil resistors feature a low temperature coefficient of resistance TCR < 2 ppm and high long term stability [Vis10]. The resistors of the low voltage part in the bottom section are of the same type but with lower resistance values.

The scale factors of the G35 divider were designed with respect to the most precise ~10 V range of the DVM. For calibration measurements using  $U_{\rm in}=1000\,{\rm V}$ , one needs a scale factor of  $M\approx 100$ : 1. To measure the maximum input voltage  $U_{\rm in}=35\,{\rm kV}$ , a scale factor of  $M\approx 3500$ : 1 is required. Additional scale factors

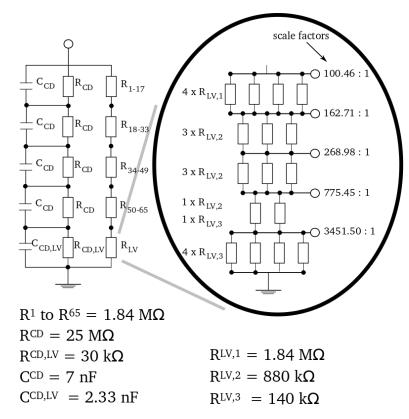


Figure 3.2: Equivalent circuit of the electrical design of the G35 divider (left) and the low voltage part  $R_{\rm LV}$  in detail (right). The corresponding values are listed below [Win18b].

are implemented to cover the whole range of possible input voltages  $U_{\rm in}$ .

The total resistance adds up to  $R_{\rm LV}\approx 1.202\,45\,{\rm M}\Omega$ . The total resistance of the upper part of the primary divider chain is  $R_{\rm HV}=65\cdot 1.84\,{\rm M}\Omega=119.6\,{\rm M}\Omega$ . A measurement of  $U_{\rm out}$  across  $R_{\rm LV}$  therefore yields a scale factor of  $M=1+119.6\,{\rm M}\Omega/1.202\,45\,{\rm M}\Omega\approx 100.46$ : 1. The other scale factors up to M=3451.5: 1 result by measuring across smaller parts of  $R_{\rm LV}$  as shown in figure 3.2 on the right. Each part of the low voltage side is realized by at least two resistors in parallel. Otherwise the breakage of a single resistor could lead to a much higher voltage across the measurement equipment and damage it.

#### 3.2.2 Control divider chain

As mentioned above, the control divider chain is a mixed ohmic/capacitive divider made of a resistor chain and a capacitor chain. The resistor chain is made of  $50 \,\mathrm{M}\Omega$  Caddock MX480 resistors with two in parallel in each section forming  $R_{\mathrm{CD}} = 25 \,\mathrm{M}\Omega$ . In the low voltage section, two in parallel connected  $10 \,\mathrm{k}\Omega$  resistors and two in parallel connected  $50 \,\mathrm{k}\Omega$  resistors of type Caddock MS260 create  $R_{\mathrm{CD,LV}}$ . The resistors of the control chain are connected to 6 copper electrodes

which can be seen in the photo of the open divider in figure 3.3, on the left. The voltage drop across the resistance  $R_{\rm CD}$  is approximately equal to the voltage across the resistors of the primary divider chain in the respective section. By design of the copper electrodes, they shield the divider chain against earth potential and furthermore form a nearly homogeneous electric field in each section, so that the potential around each resistor  $R_1$  to  $R_{65}$  has approximately the same value as the potential applied to the resistor. This shall reduce leakage currents and prevent corona discharges.

The function of the capacitive divider is the protection of the precision resistors against high voltage peaks. A sudden application of a high DC voltage includes high frequency AC parts. These would lead to a very high voltage drop across the first resistor due to stray capacitances between e.g. the copper electrodes and the sealed vessel. Therefore, a capacitor chain is added so that the control chain is being loaded instead of the precision chain. The built-in capacitors by Fischer & Tausche have a nominal value of  $2.5\,\mathrm{nF} \pm 10\%$  for voltages up to  $20\,\mathrm{kV}$ . Measurements of a single capacitor yielded  $C_{\mathrm{CD,\ LV}} \approx 2.33\,\mathrm{nF}$ .  $C_{\mathrm{CD}} \approx 7\,\mathrm{nF}$  is realized by a parallel connection of three capacitors.





**Figure 3.3:** Photos of the upper part of the open G35 divider (left) and with sealed vessel (right).

## 3.3 Mechanical setup of the G35 divider

Figure 3.3 shows a photo of the upper part of the open divider on the left and a photo of the closed divider on the right. The copper electrodes are mounted on an aluminium plate via holders made of POM<sup>3</sup>. The primary chain runs helically in the centre and is guided through holes in the electrodes with POM feedthroughs. The high voltage can be applied via a HV connector on the top electrode. The divider is enclosed by a stainless steel vessel surrounded by insulating foam. Beneath the aluminium plate is space for electronics, the digital volt meter and the water-cooling system. The temperature inside the divider is regulated by a PID slow control via 4 Pt100 sensors with  $\Delta T \leq 0.05$  °C. For optimal precision, the divider can be placed under nitrogen atmosphere and cooled to 15.0 °C but it can also be used with air and stabilization to room temperature.

<sup>&</sup>lt;sup>3</sup>polyoxymethylene

## 4 Frequency compensation

For fast voltage measurements within a time frame  $\sim 10 \,\mathrm{ms}$ , a frequency compensated divider is required. The method of frequency compensation and the possibility of its implementation at the G35 divider are discussed in section 4.1 and the following sections.

## 4.1 Theory of frequency compensation

A simple ohmic capacitive voltage divider consists of two ohmic resistances  $R_i$  with a capacitance  $C_i$  in parallel for each of them. The electric circuit diagram is shown in figure 4.1 where HV refers to the high voltage side and LV refers to the low voltage side. The frequency dependent electrical impedance  $\underline{Z}_i$  is [Ber97]:

$$\underline{Z}_{i} = \frac{\underline{Z}_{R_{i}} \cdot \underline{Z}_{C_{i}}}{\underline{Z}_{R_{i}} + \underline{Z}_{C_{i}}} = \frac{R_{i} \cdot \frac{1}{j\omega C_{i}}}{R_{i} + \frac{1}{j\omega C_{i}}} = \frac{R_{i}}{1 + j2\pi f R_{i} C_{i}},$$

$$(4.1)$$

where j is the imaginary unit and f is the frequency. The ratio of input voltage  $U_{in}$  to output voltage  $U_{out}$  is defined as the scale factor M:

$$M = \frac{U_{in}}{U_{out}} = \frac{Z_{HV} + Z_{LV}}{Z_{LV}} = 1 + \frac{Z_{HV}}{Z_{LV}}.$$
 (4.2)

With equation 4.1, M can be expressed as a term which resembles the scale factor known for DC measurements and a frequency dependent term (f.d.t):

$$M = 1 + \frac{R_{HV}}{1 + j \, 2\pi f R_{HV} C_{HV}} \cdot \frac{1 + j \, 2\pi f R_{LV} C_{LV}}{R_{LV}} \tag{4.3}$$

$$M = \underbrace{1 + \frac{R_{HV}}{R_{LV}}}_{\text{DC scale factor}} \cdot \underbrace{\frac{1 + j \, 2\pi f R_{LV} C_{LV}}{1 + j \, 2\pi f R_{HV} C_{HV}}}_{\text{frequency dependent term (f.d.t)}}.$$

The condition for a frequency compensated voltage divider is therefore that the RC time constants  $\tau$  of the high voltage and low voltage side must be equal:

$$\tau_{LV} = R_{LV}C_{LV} \stackrel{!}{=} R_{HV}C_{HV} = \tau_{HV} \quad \Rightarrow \text{f.d.t.} = 1.$$
 (4.4)

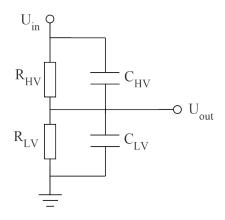


Figure 4.1: Electric circuit diagram of a simple mixed ohmic/capacitive voltage divider.

## 4.2 Frequency compensation of a test setup

We want to study the effects of frequency compensation on a test setup shown in figure 4.2. It consists of a simple voltage divider and a variable capacity  $C_{Var}$  connected to a Tektronix MSO 4054 oscilloscope and a digital volt meter (DVM) Keysight 3458A. The DVM will also later be used for the fast HV voltage measurements and is therefore added to the test setup. The Tektronix AFG3102 function generator (FG) connected to the voltage divider provides voltages in form of sinus waves or square pulses. The oscilloscope displays the input and output signal.

The electric circuit diagram of the setup is shown in figure 4.3. The function generator creates the input signal that is connected to two Caddock resistors with  $R_1 = R_2 = 1 \,\mathrm{M}\Omega$ . Resistance  $R_2$  is connected to the Keysight 3458A with an input capacitance  $C_{\mathrm{DVM}} = 267 \,\mathrm{pF}$  via a cable with  $C_{cab} \approx 130 \,\mathrm{pF}$ . We neglect

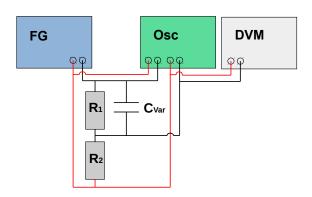


Figure 4.2: Schematic of the test setup.

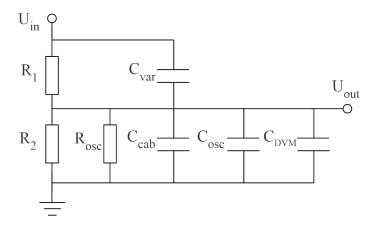


Figure 4.3: Electric circuit diagram of the test setup.

the input resistance  $R_{\rm DVM} \geq 10\,{\rm G}\Omega$ . The connection to the oscilloscope adds  $C_{osc} \approx 13\,{\rm pF}$  and  $R_{osc} = 1\,{\rm M}\Omega$ . The total resistance of the bottom part yields  $R_{meas} = (R_2 \cdot R_{osc})/(R_2 + R_{osc}) = 0.5\,{\rm M}\Omega$ . With this, the scale factor of the voltage divider is  $M = 1 + R_1/R_{\rm meas} = 3$ .

We measure the total capacitance of the bottom part with a Keysight U1732C LCR meter to be  $C_{meas} = (413 \pm 7) \,\mathrm{pF}$ . The capacitance  $C_{Var}$  in parallel to  $R_1$  can be varied by adding different ceramic capacitors.

According to equation 4.4, a compensated divider needs to fulfil

$$\tau_1 = R_1 \cdot C_{Var} = \frac{R_2 \cdot R_{osc}}{R_2 + R_{osc}} \cdot (C_{cab} + C_{osc} + C_{DVM}) = \tau_2.$$

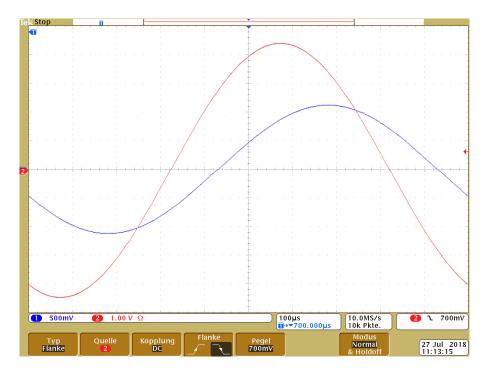
The optimal capacitance for compensation is therefore

$$C_{Var} = \frac{R_{meas}}{R_1} \cdot C_{meas} = \frac{1}{2} \cdot (413 \pm 7) \,\text{pF} = (206 \pm 4) \,\text{pF}.$$

For our measurements, the function generator creates sine waves or square pulses with a frequency  $f = 1 \,\text{kHz}$  and an amplitude  $U_{\text{out}} = 9 \,\text{V}_{\text{pp}}$ . The following figures present the results on the screen of the oscilloscope. Figures 4.4 and 4.5 show the result for a measurement without compensation by adding no ceramic capacitors, i.e.  $C_{Var} = 0$ . In figure 4.4 the generated input signal (red) is a sine wave. The output signal (blue) is delayed because the system is not compensated.

Figure 4.5 shows the result for a square pulse input signal (red). The output signal (blue) shows the characteristics of a capacitor charging because the system is not compensated.

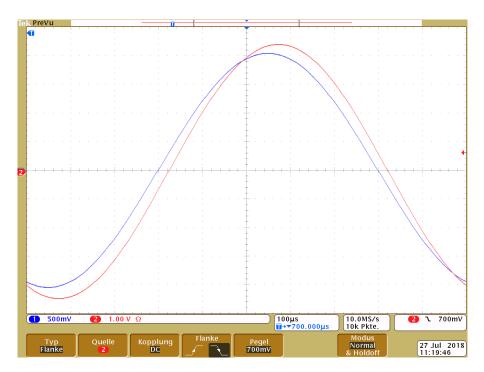
We integrate a capacitor in the system so that  $C_{Var} = 410 \,\mathrm{pF}$  to demonstrate the effects of overcompensation. Figure 4.6 shows the result for a sine wave input



**Figure 4.4:** Input signal (red) and output signal (blue) for a sine wave without compensation  $(C_{Var} = 0)$ .



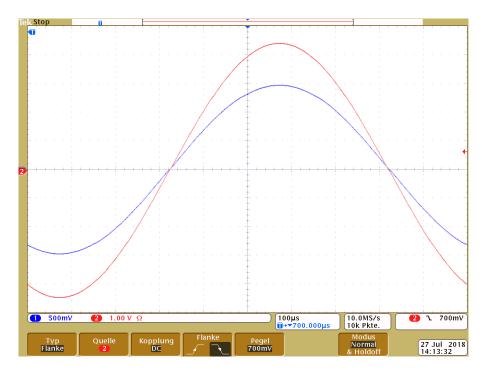
Figure 4.5: Input signal (red) and output signal (blue) for a square pulse without compensation  $(C_{Var}=0)$ .



**Figure 4.6:** Input signal (red) and output signal (blue) for a sine wave with overcompensation ( $C_{Var} = 410 \text{ pF}$ ).



Figure 4.7: Input signal (red) and output signal (blue) for a square pulse with over-compensation ( $C_{Var}=410~{\rm pF}$ ).



**Figure 4.8:** Input signal (red) and output signal (blue) for a sine wave with optimal compensation  $(C_{Var} = (204 \pm 1) \text{ pF}).$ 



Figure 4.9: Input signal (red) and output signal (blue) for a square pulse with optimal compensation  $(C_{Var}=(204\pm1)~\mathrm{pF})$ .

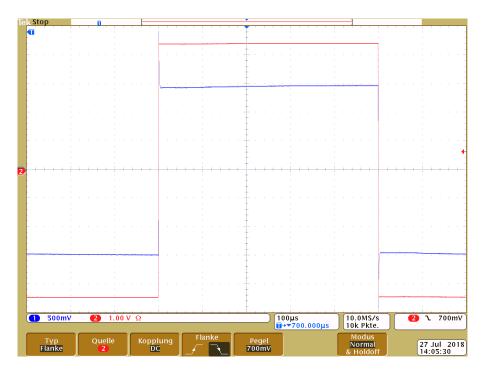


Figure 4.10: Input signal (red) and output signal (blue) for a square pulse with slight undercompensation  $(C_{Var} = (202 \pm 1) \text{ pF})$ 

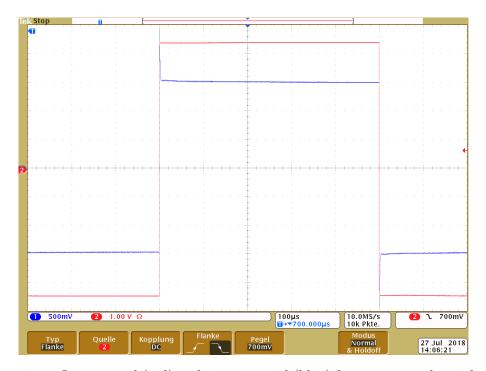


Figure 4.11: Input signal (red) and output signal (blue) for a square pulse with slight overcompensation  $(C_{Var}=(206\pm1)\,\mathrm{pF}).$ 

signal (red). The output signal (blue) runs in front of the input signal because the system is overcompensated.

Figure 4.7 shows the result for a square pulse input signal (red). The output signal (blue) shows the characteristics of a capacitor discharging because the system is overcompensated.

For optimal compensation, we integrate a 200 pF ceramic capacitor and a Sprague-Goodman GAA6R004 trimmer capacitor of  $C_{tr} = 0.6 \,\mathrm{pF} - 6 \,\mathrm{pF}$  in parallel so that  $C_{Var}$  can be tuned to values between 200.6 pF and 206 pF. Figures 4.8 and 4.9 show the results for optimal compensation which we find for  $C_{Var} = (204 \pm 1) \,\mathrm{pF}$ . Figure 4.8 shows the alignment of zero-crossings and peaks of input and output signal as we expect it for optimal compensation. The output voltage is  $U_{out} \approx 3 \,\mathrm{V_{pp}}$ , so that the scale factor  $M = U_{\rm in}/U_{\rm out} = 9/3 = 3$  is as expected. Figure 4.9 shows the nearly immediate response of the output signal without rise or decay that is expected with optimal compensation. We attribute the small peak at the start of the output signal to slight instabilities in the setup that cannot be reduced further. Figures 4.10 and 4.11 show results for slight undercompensation with  $C_{Var} = (202 \pm 1) \,\mathrm{pF}$  and slight overcompensation  $C_{Var} = (206 \pm 1) \,\mathrm{pF}$ .

## 4.3 Frequency compensation of the G35 Divider

The possibility of a frequency compensation of the G35 divider was studied for the first time by T. Dirkes in his bachelor thesis [Dir17]. This included measurements on a test setup similar to the G35 divider. During maintenance and reconstruction of the KATRIN K65 divider, he installed a frequency compensation on a partial setup which featured three copper electrodes and a scale factor of  $M\approx 21$ . Although the G35 divider with 6 copper electrodes is twice as large, the test setup was very similar in terms of the design and structure. Figure 4.12 shows his results. Due to the connection of an oscilloscope with  $R_{\rm int}=1\,{\rm M}\Omega$ , the effective DC scale factor was  $M\approx 50$ . The best compensation for all frequencies between 10 Hz and  $10^5\,{\rm Hz}$  was reached for  $\tau=R_{\rm HV}\cdot C_{\rm HV}=29\,{\rm M}\Omega\cdot 90\,{\rm pF}\approx 2.61\,{\rm ms}$ . No satisfactory compensation could be achieved for smaller capacitances. A possible cause why the divider could not be compensated with capacitances  $C_{\rm HV}<90\,{\rm pF}$ , are stray capacitances of the divider with high enough values to influence the compensation.

If this behaviour can be transferred to the G35 divider,  $C_{\rm HV,G35}$  needs to be in the order of 100 pF as well. This means  $\tau_{\rm G35} = C_{\rm HV,G35} R_{\rm HV,G35} = 100 \, \rm pF \cdot 119.6 \, M\Omega \approx 12 \, \rm ms$ . Because  $\tau > 10 \, \rm ms$  which is the time frame for the measurement, the compensation has to be very precise and stable to ensure that the system is

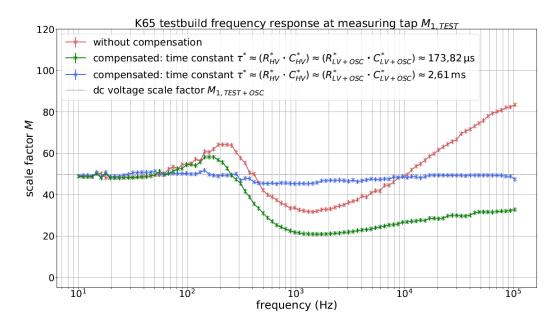


Figure 4.12: Measurements of a frequency compensated test setup with DC scale factor  $M \approx 50$  [Dir17].

compensated fast enough and the desired accuracy is reached. This is further investigated in this thesis by simulating the system in LT Spice.

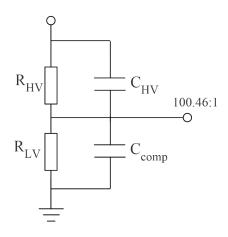
#### 4.3.1 LT Spice simulations of the compensated G35 divider

Simulations of the compensated G35 divider with  $C_{\rm HV}=100\,{\rm pF}$  were done in LT Spice via a transient analysis. The equivalent circuit diagram is shown in figure 4.13. The compensated lower voltage part with  $R_{\rm LV}=1.202\,451\,{\rm M}\Omega$  corresponds to the scale factor M=100.46. With equation 4.4 follows for the low voltage capacitance:

$$C_{\text{LV}} = \frac{R_{\text{HV}}}{R_{\text{LV}}} \cdot C_{\text{HV}} = 9.94635 \,\text{nF}$$
  
 $C_{\text{comp}} = C_{\text{LV}} - C_{\text{meas}} = 9.40135 \,\text{nF}$ 

where  $C_{\text{meas}} = 545 \,\text{pF}$  includes the capacitances of the DVM and the cables.

The transient analysis was performed by applying a pulse of  $U_{\rm in}=1\,\rm kV$  to the system and simulating the response for a time of 20 ms. The slew rate of the pulse was chosen to be 12 V/µs which is the slew rate of the *Kepco* Bop1000m amplifier available in our group. The expected DC output voltage for M=100.46 is  $U_{\rm out,DC}=1\,\rm kV/100.46=9.953\,86\,V$ . For a compensation that fulfils the require-



**Figure 4.13:** Equivalent electric circuit diagram of the G35 divider.

ments, this value must be reached within 10 ms<sup> 1</sup> with an accuracy of 10 ppm.

By varying  $C_{\rm comp}$  and  $C_{\rm HV}$  in separate simulations, we test how sensitive the compensation is to deviations of the capacitances. The results for the variation of  $C_{\rm comp}$ , while  $C_{\rm HV}=100\,{\rm pF}$  is kept constant, are shown in figures 4.14 and 4.15. The blue bands mark the area of  $U_{\rm out,\ DC}\pm\Delta U_{\rm out,\ DC}$  for  $\Delta U_{\rm out,\ DC}=100\,{\rm ppm}$  and  $\Delta U_{\rm out,\ DC}=10\,{\rm ppm}$ .

The case of perfect compensation is given by the green curves (sim 3) in both plots where the expected value  $U_{\rm out} = 9.953\,86\,\mathrm{V}$  is reached instantaneously with respect to the slew rate. The yellow (sim 2) and red (sim 4) curves in figure 4.14 show that deviations of  $C_{\rm comp}$  may not be bigger than  $\Delta C_{\rm comp} = 2.35\,\mathrm{pF} \,\hat{=}\, \Delta C_{\rm comp}/C_{\rm comp} = 2.5\cdot 10^{-4}$  to reach an accuracy of 100 ppm in 10 ms. Deviations of  $\Delta C_{\rm comp} = 4.7\,\mathrm{pF} \,\hat{=}\, \Delta C_{\rm comp}/C_{\rm comp} = 5\cdot 10^{-4}$  allow to achieve 100 ppm accuracy in 20 ms, represented by the blue (sim 1) and purple (sim 5) curves.

The deviations to reach the required 10 ppm accuracy can be taken from figure 4.15. The yellow (sim 2) and red (sim 4) curves show that deviations of  $C_{\text{comp}}$  may not be bigger than  $\Delta C_{\text{comp}} = 0.24 \,\text{pF} = \Delta C_{\text{comp}}/C_{\text{comp}} = 2.5 \cdot 10^{-5}$  to reach 10 ppm accuracy in 10 ms. Deviations of  $\Delta C_{\text{comp}} = 0.47 \,\text{pF} = \Delta C_{\text{comp}}/C_{\text{comp}} = 5 \cdot 10^{-5}$  allow to achieve 10 ppm accuracy in 20 ms, as can be seen in the blue (sim 1) and purple (sim 5) curves.

Figures 4.16 and 4.17 show the results for the variation of  $C_{\rm HV}$ , while  $C_{\rm comp} = 9.401\,35\,\rm nF$  is kept constant. The relative deviations to achieve certain accuracies are the same, e.g. they must be smaller than  $\Delta C_{\rm HV} = 0.025\,\rm pF \,\,\hat{=}\,\, \Delta C_{\rm HV}/C_{\rm HV} = 2.5\cdot 10^{-5}$  to reach 10 ppm accuracy in 10 ms as well.

<sup>&</sup>lt;sup>1</sup>neglecting the integration time of the DVM for now.

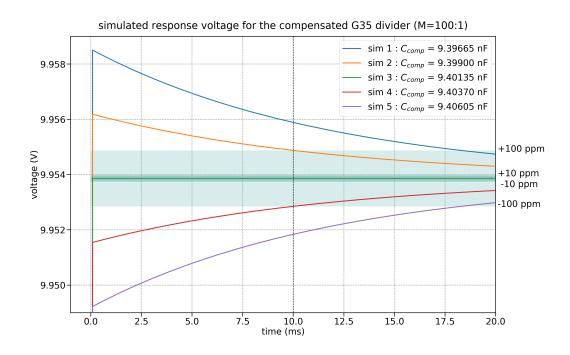


Figure 4.14: Simulated response voltages of the compensated G35 divider (M = 100.46:1) to a 1 kV input pulse for varied capacitances  $C_{\text{comp}}$ .

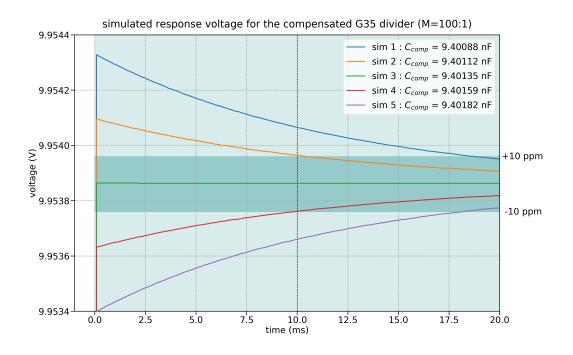


Figure 4.15: Simulated response voltages of the compensated G35 divider (M = 100.46:1) to a 1 kV input pulse for varied capacitances  $C_{\text{comp}}$ .

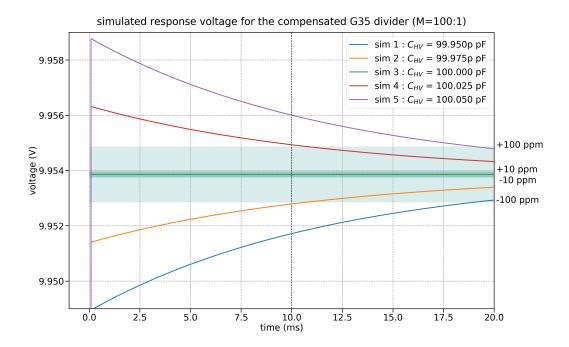


Figure 4.16: Simulated response voltages of the compensated G35 divider (M = 100.46:1) to a 1 kV input pulse for varied capacitances  $C_{\rm HV}$ .

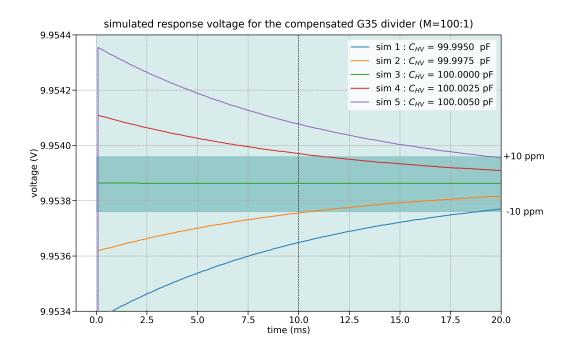


Figure 4.17: Simulated response voltages of the compensated G35 divider (M = 100.46:1) to a 1 kV input pulse for varied capacitances  $C_{\rm HV}$ .

### 4.3.2 Discussion and consequences of simulation results

The simulation results make a frequency compensation of the G35 divider that complies with the requirements unrealistic. The necessary stability of  $\Delta C = 2.5 \cdot 10^{-5}$  can hardly be achieved with available capacitors. In addition, the design of the G35 divider is not laid out for frequency compensation, which would require a modification of the working system. For these reasons, the plan of a frequency compensation of the G35 divider was not pursued further. Instead, it is proposed to build a separate, fast voltage divider complementing the G35 divider. The requirements on the long term stability of this add-on divider could be relaxed compared to the G35, as the latter can be used for calibration of the smaller frequency compensated divider before and after measurements.

The fast divider would therefore allow the use of smaller capacitances for compensation due to smaller stray capacitances. With a smaller time constant, the capacitances for compensation would have to be less stable to meet the requirements. The design of the fast divider is presented in Chapter 5.

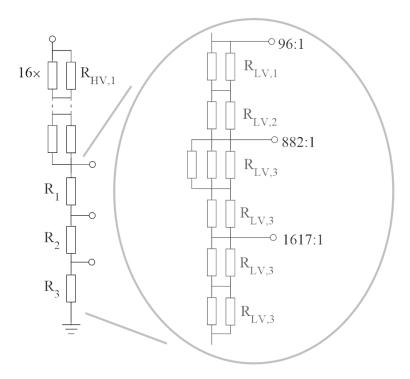
## 5 Design of a new fast voltage divider

The construction of a new frequency compensated HV divider was proposed for the reasons discussed in chapter 4. By pursuing a compact design, stray capacitances will be reduced in comparison to the G35 divider. As mentioned in section 4.3.2, this new divider will have relaxed requirements regarding long-term stability and will use the readout electronics of the G35 divider. It will therefore be operated as an add-on to the existing divider. Such a design will allow the usage of smaller capacitances which leads to a faster frequency compensation. This chapter presents the electrical design including calculations of the necessary capacitance values as well as the mechanical design of the divider.

## 5.1 Electrical design and LT-Spice simulations

The equivalent circuit of the primary divider chain is shown in figure 5.1. Caddock USF371 type resistors with  $R_{\rm HV,1}=20\,{\rm M}\Omega$  will be used. These resistors have a temperature coefficient of 5 ppm/K and a voltage coefficient of 0.02 ppm/V. The maximum voltage across a single resistor must not exceed 2500 V. As the new divider is planned as a supplement to the G35 divider, its maximum input voltage shall be  $U_{\rm in,max}=35\,{\rm kV}$  as well. Hence, a number of  $>35\,{\rm kV}/2.5\,{\rm kV}>14$  resistors in series is at least needed for the high voltage side. To increase the current, the total resistance is reduced by using 16 in parallel connected pairs of resistors. Its total resistance is  $R_{\rm HV}=160\,{\rm M}\Omega$ .

The lower voltage side contains  $R_{\text{LV},1} = 2 \,\text{M}\Omega$ ,  $R_{\text{LV},2} = 1 \,\text{M}\Omega$  and  $R_{\text{LV},3} = 100 \,\text{k}\Omega$  Caddock USF340 resistors. As for the G35 divider, each part of the low voltage side is realized by at least two resistors in parallel to protect the measurement equipment against harmful high voltages in case of a breakage of a single resistor. The three output connections realize the scale factors  $M = 96 \, (100:1)$ ,  $M = 882 \, (900:1)$  and  $M = 1617 \, (1600:1)$ . They are chosen according to the necessary cooling voltages discussed in section 2.3.1. Cooling voltages up to 16.4 kV are needed in principle and can be measured most precisely using the 1600:1 scale factor. The 900:1 scale factor can be used for voltages of about 8 kV which are sufficient for heavy ion experiments plus additional detuning voltages  $\pm 2 \,\text{kV}$  for the dielectronic recombination experiments. The 100:1 scale factor will be used for the calibration of the divider.



**Figure 5.1:** Equivalent circuit diagram of the primary divider chain with  $R_{\rm HV,1} = 20\,{\rm M}\Omega$  (left) and the low voltage part in detail (right) with  $R_{\rm LV,1} = 2\,{\rm M}\Omega$ ,  $R_{\rm LV,2} = 1\,{\rm M}\Omega$  and  $R_{\rm LV,3} = 100\,{\rm k}\Omega$ .

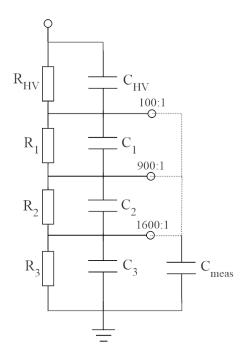
#### 5.1.1 Calculation of capacitances for compensation

Figure 5.2 shows an equivalent circuit of the divider which is used to determine the capacitances needed for the frequency compensation. The lower voltage resistor chain can be split into the resistances  $R_1 = 1.5 \,\mathrm{M}\Omega$ ,  $R_2 = 83.\overline{3}\,\mathrm{k}\Omega$  and  $R_3 = 100\,\mathrm{k}\Omega$ .

To achieve the best frequency compensation, the high voltage capacitance  $C_{\rm HV}$  parallel to  $R_{\rm HV}$  will have the smallest possible value which depends on the capacitance of the measurement equipment  $C_{\rm meas}$ . We assume a capacitance of  $C_{\rm meas} = 500\,{\rm pF}$  including the input capacitance of the Keysight 3458A  $C_{\rm DVM} = 267\,{\rm pF}$ . This leaves a capacitance of  $C = 233\,{\rm pF}$  for the measurement cable with  $C_{\rm cab}$  and a trimming capacitor with  $C_{\rm trim}$  to ensure the value is as close to 500 pF as possible. With this, the minimal value for  $C_{\rm HV} = 6\,{\rm pF}$  so that

$$\tau_{\rm HV} = 6 \,\mathrm{pF} \cdot 160 \,\mathrm{M}\Omega = 0.96 \,\mathrm{ms}.$$
 (5.1)

The capacitances  $C_1$ ,  $C_2$  and  $C_3$  for compensation of the lower voltage side depend on which scale factor is used, i.e. where the measurement equipment is connected.



**Figure 5.2:** Equivalent circuit diagram of the fast divider.

As indicated in figure 5.2, connecting the output to the DVM means connecting  $C_{\text{meas}}$  in parallel to the low voltage part, i.e. forming a RC element which needs to fulfil  $R \cdot C = \tau_{\text{HV}}$ . Hence,  $C_1$ ,  $C_2$  and  $C_3$  have to differ for compensation of the 100:1, 900:1 and 1600:1 scale factor. They can be calculated using the following conditions that need to be fulfilled for compensation.

**Compensation of 100:1** Each RC element of the low voltage side containing  $R_1$ ,  $R_2$  or  $R_3$  has to be compensated with each other for the 100:1 scale factor with a time constant  $\tau_{100}^*$ . The time constant  $\tau_{100}^* \neq \tau_{HV}$  though, because  $C_{\text{meas}}$  is not yet included.

$$\tau_{100}^* = R_1 \cdot C_{1,100} = R_2 \cdot C_{2,100} = R_3 \cdot C_{3,100} \Leftrightarrow$$

$$C_{1,100} = \frac{R_3}{R_1} \cdot C_{3,100} \quad \text{and} \quad C_{2,100} = \frac{R_3}{R_2} \cdot C_{3,100}$$
(5.2)

During a measurement, the lower voltage side with a total capacitance  $C_{123}$  including  $C_{\text{meas}}$  has to be compensated such that  $\tau_{100} = \tau_{\text{HV}}$ :

$$C_{123} = C_{\text{meas}} + \left(\frac{1}{C_{1,100}} + \frac{1}{C_{2,100}} + \frac{1}{C_{3,100}}\right)^{-1}$$

$$\tau_{100} = (R_1 + R_2 + R_3) \cdot C_{123} \stackrel{!}{=} \tau_{\text{HV}}$$
(5.3)

Applying equation 5.2 to 5.3 yields:

$$\frac{\tau_{\text{HV}}}{R_1 + R_2 + R_3} = C_{\text{meas}} + C_{3,100} \left(\frac{R_1}{R_3} + \frac{R_2}{R_3} + 1\right)^{-1} \Leftrightarrow C_{3,100} = \left(\frac{\tau_{\text{HV}}}{R_1 + R_2 + R_3} - C_{\text{meas}}\right) \cdot \left(\frac{R_1}{R_3} + \frac{R_2}{R_3} + 1\right).$$
(5.4)

With equations 5.2 and 5.4 the capacitances for the compensation of the 100:1 scale factor can be calculated.

**Compensation of 900:1** For the 900:1 scale factor,  $R_1 \cdot C_{1,900}$  is independent of  $C_{\text{meas}}$  and needs to be compensated to become equal to  $\tau_{\text{HV}}$ . The other two RC elements with  $\tau_{900}^*$  need to be compensated with each other:

$$R_1 \cdot C_{1,900} \stackrel{!}{=} \tau_{HV} \Leftrightarrow C_{1,900} = \frac{\tau_{HV}}{R_1}$$
 (5.5)

$$\tau_{900}^* = R_2 \cdot C_{2,900} = R_3 \cdot C_{3,900} \Leftrightarrow C_{2,900} = \frac{R_3}{R_2} \cdot C_{3,900}$$
 (5.6)

The condition for compensation of  $C_{2,900}$  and  $C_{3,900}$  including  $C_{\text{meas}}$  is:

$$C_{23} = C_{\text{meas}} + \left(\frac{1}{C_{2,900}} + \frac{1}{C_{3,900}}\right)^{-1}$$

$$\tau_{900} = (R_2 + R_3) \cdot C_{23} \stackrel{!}{=} \tau_{\text{HV}}.$$
(5.7)

With equation 5.6 follows:

$$\frac{\tau_{\text{HV}}}{R_2 + R_3} = C_{\text{meas}} + C_{3,900} \left(\frac{R_2}{R_3} + 1\right)^{-1} \Leftrightarrow C_{3,900} = \left(\frac{\tau_{\text{HV}}}{R_2 + R_3} - C_{\text{meas}}\right) \cdot \left(\frac{R_2}{R_3} + 1\right).$$
(5.8)

With equations 5.5, 5.6 and 5.8 the capacitances for the compensation of the 900:1 scale factor can be calculated.

**Compensation of 1600:1** For the 1600:1 scale factor,  $R_1 \cdot C_{1,1600}$  and  $R_2 \cdot C_{2,1600}$  need to be compensated to obtain the time constant  $\tau_{HV}$ :

$$R_1 \cdot C_{1,1600} = R_2 \cdot C_{2,1600} \stackrel{!}{=} \tau_{HV} \Leftrightarrow$$

$$C_{1,1600} = \frac{\tau_{HV}}{R_1} = C_{1,900} \quad \text{and} \quad C_{2,1600} = \frac{\tau_{HV}}{R_2}.$$
(5.9)

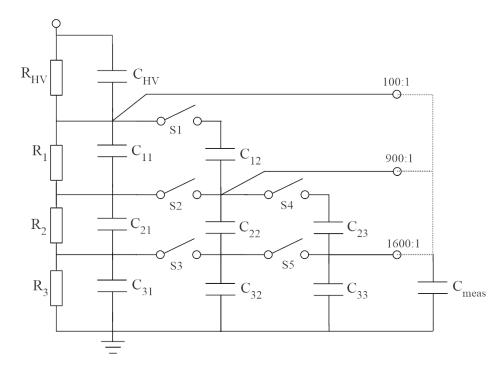


Figure 5.3: Equivalent circuit diagram of the frequency compensated divider.

The condition for compensation of  $C_{3,1600}$  including  $C_{\text{meas}}$  is:

$$\tau_{1600} = (C_{3,1600} + C_{\text{meas}}) \cdot R_3 \stackrel{!}{=} \tau_{\text{HV}} \Leftrightarrow$$

$$C_{3,1600} = \frac{\tau_{\text{HV}}}{R_3} - C_{\text{meas}}.$$
(5.10)

With equations 5.9 and 5.10 the capacitances for the compensation of the 1600:1 scale factor can be calculated.

#### 5.1.2 Technical realization

The compensation of the lower voltage side is realized with an electric circuit containing capacitances  $C_{ij}$  as shown in figure 5.3. Switches connecting the capacitances allow to realize the required capacitances calculated in section 5.1.1 for the different scale factors. For the 100:1 scale factor, all switches are open and the compensation is carried out by capacitances  $C_{11}$ ,  $C_{21}$  and  $C_{31}$  representing  $C_{i,100}$ , i = 1, 2, 3. For the 900:1 scale factor,  $C_{12}$ ,  $C_{22}$  and  $C_{32}$  will be added by closing switches S1, S2 and S3 to reach the values  $C_{i,900}$ . By closing switches S4 and S5,  $C_{23}$  and  $C_{33}$  will be added to get to  $C_{i,1600}$ . The capacitances  $C_{ij}$  therefore need to have the values shown in table 5.1. The switch positions for the usage of the different scale factors are listed in table 5.2.

Each capacitance  $C_{ij}$  will be realized by a mix of capacitors to get as close as possible to the optimal value. Deviations due to temperature variations are com-

$C_{11} = C_{1,100}$	$C_{12} = C_{1,900} - C_{1,100}$	$C_{13} = C_{1,1600} - C_{1,900} = 0$
$C_{21} = C_{2,100}$	$C_{22} = C_{2,900} - C_{2,100}$	$C_{23} = C_{2,1600} - C_{2,900}$
$C_{31} = C_{3,100}$	$C_{32} = C_{3,900} - C_{3,100}$	$C_{33} = C_{3,1600} - C_{3,900}$

$C_{11} = 78.89 \mathrm{pF}$	$C_{12} = 561.11 \mathrm{pF}$	$C_{13} = 0$
$C_{21} = 1.42000 \mathrm{nF}$	$C_{22} = 9.00000 \mathrm{nF}$	$C_{23} = 1.10000 \mathrm{nF}$
$C_{31} = 1.18333 \mathrm{nF}$	$C_{32} = 7.50000 \mathrm{nF}$	$C_{33} = 416.67 \mathrm{pF}$

**Table 5.1:** Calculation of capacitances  $C_{ij}$  shown in figure 5.3 and their respective values for  $C_{HV} = 6 \,\mathrm{pF}$  and  $C_{\mathrm{meas}} = 500 \,\mathrm{pF}$ .

pensated by additional trimming capacitors. Three of these are included in capacitances  $C_{11}$ ,  $C_{21}$  and  $C_{31}$ . After connecting  $C_{\text{meas}}$  and setting the switches, the balancing of  $C_{\text{LV}}$  can be controlled by trimming  $C_{11}$ ,  $C_{21}$  and  $C_{31}$ . As these are part of the compensation for all three scale factors, trimming of  $C_{11}$ ,  $C_{21}$  and  $C_{31}$  is sufficient to equalize deviations in other  $C_{ij}$ .

	100:1	900:1	1600:1
S1	off	on	on
S2	off	on	on
S3	off	on	on
S4	off	off	on
S5	off	off	on

Table 5.2: Switch positions for the compensation of different scale factors.

#### 5.1.3 LT spice simulations

The electric circuit of the divider shown in figure 5.3 was simulated in LT spice. The calculated values for  $C_{ij}$  in table 5.1 are applied to test how sensitive the system is towards deviations of the capacitances. In particular, it is of interest how far the capacitances may deviate in order to still enable a voltage measurement with 10 ppm accuracy with the *Keysight* 3458A DVM. In the fast  $6\frac{1}{2}$  digit mode, which allows an accuracy of 10 ppm, the minimum integration time of the DVM is  $\approx 1.7 \,\text{ms}$  [Key14].

The transient analysis method is similar to the simulations of the G35 divider discussed in section 4.3.1. A pulse of  $U_{\rm in}=1\,\rm kV$  with a slew rate of  $12\,\rm V/\mu s$  was applied to the system. All switches are open, so that the scale factor is M=96.04 and the expected DC value is  $U_{\rm out,\ DC}=10.411\,30\,\rm V$ . Figure 5.4 shows the results for variation of  $C_{11}$  while all other capacitances are kept at

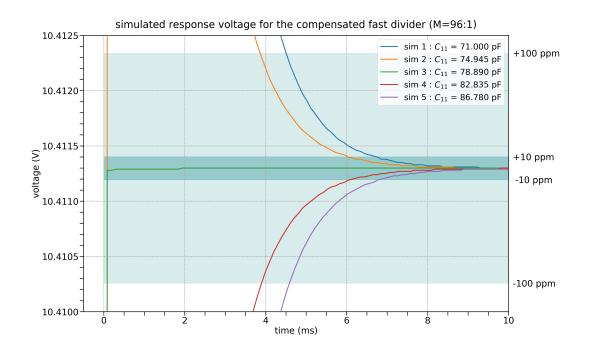


Figure 5.4: Simulated response voltages of the compensated new fast divider (M = 100:1) to a 1 kV input pulse for varied capacitances  $C_{11}$ 

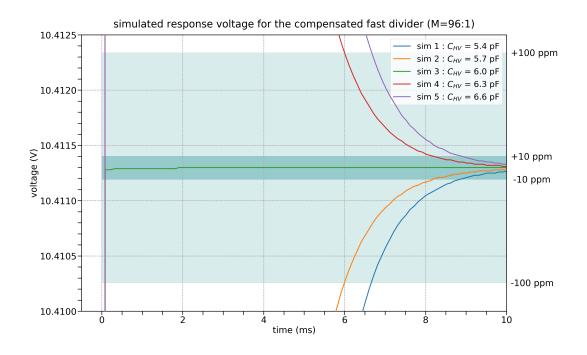


Figure 5.5: Simulated response voltages of the compensated new fast divider (M = 100:1) to a 1 kV input pulse for varied capacitances  $C_{HV}$ 

their perfect values. The green curve (sim 3) represents the case of perfect compensation where  $U_{\rm out,\ DC}$  is reached almost instantaneously. The yellow (sim 2) and red curve (sim 4) show that the required accuracy of 10 ppm is achieved after  $\approx 6 \,\mathrm{ms}$  for deviations  $\Delta C_{11} = 3.945 \,\mathrm{pF} \,\hat{=}\, 5\%$  and after  $\approx 6.7 \,\mathrm{ms}$  for deviations  $\Delta C_{11} = 7.889 \,\mathrm{pF} \,\hat{=}\, 10\%$ .

Figure 5.5 shows the results for variation of  $C_{\rm HV}$  while all other capacitances are kept at their perfect values. The yellow (sim 2) and red curve (sim 4) show that the required accuracy of 10 ppm is achieved after  $\approx 8.2\,\rm ms$  for deviations  $\Delta C_{\rm HV} = 0.3\,\rm pF \, \hat{=}\, 5\%$  and after  $\approx 8.8\,\rm ms$  for deviations  $\Delta C_{\rm HV} = 0.6\,\rm pF \, \hat{=}\, 10\%$ .

Summing up, the simulations show that for deviations of capacitance  $C_{11}$  up to 10%, the compensation is fast enough to leave time for a measurement with an accuracy of 10 ppm. For  $C_{HV}$ , deviatons of up to 5% are acceptable. Such a compensation can be achieved by a combination of commercially available capacitors and additional trimming capacitors. With the latter, fluctuations due to temperature and environment will be corrected. We therefore assume that the requirements can be achieved with this realization of the frequency compensation.

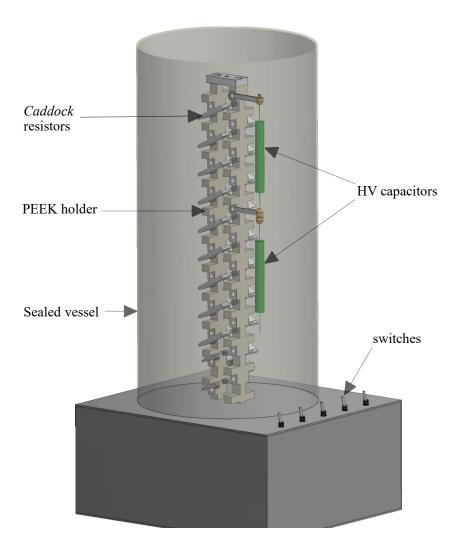
## 5.2 Mechanical design

Figure 5.6 shows a preliminary 3D CAD model of the fast voltage divider. It will be much smaller than the G35 divider and has no copper electrodes. Therefore, the stray capacitances are expected to be much smaller. The Caddock resistors are installed on a PEEK<sup>1</sup> holder. Two capacitors in green are shown which form  $C_{\rm HV}$ . The capacitances for compensation of the low voltage side will be installed on a circuit board in the box below the divider chain. The five switches used to set the correct compensation for the chosen scale factor can be seen on top of the box. The finished divider setup will have additional switches in the circuit used for connection to the measurement devices. The divider is enclosed by a sealed stainless steal vessel as a Faraday shield which is kept transparent in the picture to make the inner divider chain visible.

#### 5.2.1 Integrated connections to DVM or oscilloscope

For the compensation to work, it is essential to reduce and control all additional capacitances in the system. Considering this, cables and connectors contribute non-negligible stray capacitances in our measurement setup. Therefore, it is planned to use fixed cables for connections wherever possible and use plugs only

<sup>&</sup>lt;sup>1</sup>Polyether ether ketone



**Figure 5.6:** Preliminary 3D model of the new fast voltage divider. The low voltage side of the divider is continued in the box at the bottom.

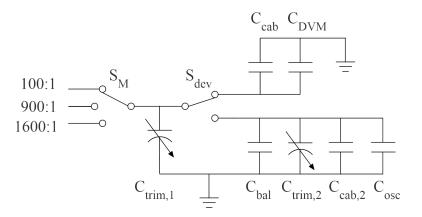


Figure 5.7: Electric circuit diagram of  $C_{\rm meas}$  in detail, with switch  $S_{\rm M}$  to choose the scale factor and switch  $S_{\rm dev}$  to choose the device.

for connections to the DVM and an oscilloscope. Hence, the use of plugs shall be avoided by installing additional switches. Figure 5.7 shows the layout of the electric circuit with the relevant capacitances for connecting the divider with the measurement equipment. The equivalent value for all capacitances in figure 5.7 is  $C_{\rm meas}$  (cf. figure 5.3). The scale factor is chosen by switch  $S_{\rm M}$  whereas switch  $S_{\rm dev}$  connects the divider to either the Keysight 3458A DVM with  $C_{\rm DVM}=267\,{\rm pF}$  or to an oscilloscope, e.g. Tektronix MSO 4054 with  $C_{\rm osc}\approx 13\,{\rm pF}$ . The total capacitance must be  $C_{\rm meas}=500\,{\rm pF}$  for both cases. The difference is therefore balanced by additon of  $C_{\rm bal}$ . A trimming capacitor  $C_{\rm trim,2}$  allows to compensate if another oscilloscope with a different capacitance is used. Trimming capacitor  $C_{\rm trim,1}$  is used for fine tuning to get as close as possible to  $C_{\rm meas}=500\,{\rm pF}$  for an optimal frequency compensation.

## 6 Conclusion

Fast precision high voltage measurements are needed for dielectronic recombination measurements at CRYRING@ESR. This thesis studied the feasibility of implementing a frequency compensation for the G35 divider based on initial investigations by T. Dirkes [Dir17]. The limitations that were found led to the proposal to build a separate fast voltage divider complementing the G35 divider. With this combined HV setup, the fast voltage measurements can presumably be performed with the desired accuracy.

Dielectronic recombination experiments have specific requirements for HV measurements, as presented in chapter 2. In these experiments, voltages of the electron cooler need to be measured with an accuracy of 10 ppm within 10 ms. The electron cooler voltage can reach  $U_{\rm cool}=16.4\,\rm kV$  in principle, while voltages  $U_{\rm cool}\leq 8\,\rm kV$  with additional detuning voltages  $\pm 2\,\rm kV$  are sufficient for experiments with heavy, highly charged ions.

Measurements on a test setup successfully demonstrated the effects of frequency compensation as described in section 4.2. By installing appropriate capacitors that ensure that  $\tau_{\rm HV} = R_{\rm HV} \cdot C_{\rm HV} = \tau_{\rm LV} = R_{\rm LV} \cdot C_{\rm LV}$ , the system could be compensated which was verified with an oscilloscope. Section 4.3 dealt with the frequency compensation of the G35 divider. Results of T. Dirkes showed that a capacitance of  $C_{\rm HV,G35}$  in the order of 100 pF is necessary for a compensation of the G35 divider, probably due to stray capacitances. Building on these results, this thesis examined a possible technical implementation. Simulated transient analyses of the electric circuit of the G35 divider were performed with LT Spice. In order to meet the measurement requirements of an accuracy of 10 ppm within 10 ms, the accuracy of the capacitances must be better than  $\Delta C = 2.5 \cdot 10^{-5}$ . This can hardly be achieved with commercially available capacitors. Therefore, the construction of a separate divider complementing the G35 divider is proposed.

The new divider has less strict specifications for long-term stability, since the G35 divider is available to calibrate the new divider before and after measurements. This allows a more compact design with smaller stray capacitances. Thus, a frequency compensation meeting the requirements can be realized, as shown in section 5.1. After deducting the integration time of the DVM, the 10 ppm accuracy of the output voltage must be achieved within 8.3 ms. The necessary accuracy

of the compensation capacitances was investigated via transient analyses of the electric circuit of the fast divider. Concluding, the capacitance for compensation  $C_{11}$  may deviate by  $\Delta C_{11} = 10\%$ . On the high voltage side, the deviations may be  $\Delta C_{HV} = 5\%$ . Such a compensation can be achieved by a combination of commercially available capacitors and additional trimming capacitors. The latter will allow readjustment and further improvement of the compensation.

The preliminary mechanical design of the additional divider was presented in 5.2. The proposed design intentionally avoids unnecessary cables and plugs to achieve minimal stray capacitances and a stable compensation.

Future proceedings include the construction of the primary divider, which is supposed to achieve a precision below 10 ppm after calibration. Subsequently, the capacitors for the frequency compensation will be installed. The quality of the frequency compensation can be tested by measurements with the *Kepco* Bop1000m amplifier in Münster.

Finally, the fast divider will be transferred to CRYRING@ESR. It will be installed next to the G35 divider. The new combined HV setup will then enable high-precision dielectronic recombination experiments.

## References

- [Bau13] S. Bauer et al.: 2013 JINST8 P10026. https://doi.org/10.1088/1748-0221/8/10/P10026
- [Ber97] K. Bergmann: Elektrische Meßtechnik: Elektrische und elektronische Verfahren, Anlagen und Systeme, 6. Auflage, Vieweg. 1997
- [BLS14] C. Brandau, M. Lestinsky, S. Schippers: Collision spectroscopy at the CRYRING@ESR electron cooler. In: Technical Design Report: Experimental Instrumentation of CRYRING@ESR, Chapter 3. 2014.
- [Bra08] C. Brandau et al. Phys. Rev. Lett. 100 (2008) 073201. https://doi.org/10.1103/PhysRevLett.100.073201
- [Cad17] Type USF Ultra-Stable Low TC Film Resistors 200 Series and 300 Series, Caddock electronics, inc., datasheet. 2017
- [Dan11] H. Danared et al.: LSR Low-energy Storage Ring Technical Design Report. 2011
- [Dir17] T. Dirkes: Design einer Frequenzkompensation des 35kV-Präzisionshochspannungsteilers für den CRYRING@ESR an der GSI/FAIR, Bachelor thesis, WWU Münster, 2017
- [Fai19] FAIR/GSI, www.fair-center.eu, viewed 7 April 2019
- [Gei17] W. Geithner et al. Hyperfine Interact (2017) 238: 13. https://doi.org/10.1007/s10751-016-1383-5
- [Hos17] J. Hosan/GSI Helmholtzzentrum für Schwerionenforschung GmbH, digital image. 2017.
- [Key14] Keysight 3458A Multimeter, data sheet. 2014
- [Les08] M. Lestinsky et al. Phys. Rev. Lett. 100 (2008) 033001. https://doi.org/10.1103/PhysRevLett.100.033001
- [Les14] M. Lestinsky et al.: Technical Design Report: Experimental Instrumentation of CRYRING@ESR. 2014.

- [Les16] Lestinsky, M. et al.: Physics book: CRYRING@ESR, Eur. Phys. J. Spec. Top. (2016) 225: 797. https://doi.org/10.1140/epjst/e2016-02643-6
- [Mül08] A. Müller, Adv. At. Mol. Opt. Phys. 55 (2008) 293. https://doi.org/10.1016/S1049-250X(07)55006-8
- [NIST] https://physics.nist.gov/cuu/Constants/index.html, viewed 19 April 2019
- [Sch14] S. Schippers: Nucl. Instr. Meth. B 350 (2015) 61–65.
- [Sch05] R. Schuch et al. Phys. Rev. Lett. 95 (2005) 183003 10.1103/Phys-RevLett.95.183003
- [Stö14] Stöhlker, T., Litvinov, Y.A., Bräuning-Demian, A. et al.: Hyperfine Interact (2014) 227: 45. https://doi.org/10.1007/s10751-014-1047-2
- [Vis10] VISHAY VHA518-11 data sheet. http://www.vishaypg.com/docs/63006/hmetlab.pdf, viewed 14 April 2019
- [Vol15] J. Vollbrecht et al.: J. Phys.: Conf. Ser.583 012002, 2015. https://doi.org/10.1088/1742-6596/583/1/012002
- [Win18a] D. Winzen: Commissioning of a detection system for forward emitted XUV photons at the ESR. DPG spring meeting, talk. 2018
- [Win18b] D. Winzen et al.: Frequency compensation and status update of the precision high voltage divider for the electron cooler at CRYRING@ESR. APPA and R&D Collaboration meeting 2018 Poster. 2018

# List of Figures

2.1	Electric field strength in highly charged ions compared to the Her-	
	cules laser [Win18a]	3
2.2	Layout of new FAIR facilities and existing GSI facilities and the	
	position of CRYRING [Gei17]	4
2.3	Overview of the CRYRING@ESR setup [Gei17]	5
2.4	Schematic of the electron cooler of CRYRING [Dan11]	6
2.5	Photos of the CRYRING setup (left) and a close up of the electron	
	cooler (right) [Hos17]	8
2.6	Principle of dielectronic recombination [Les14]	Ć
2.7	Schematic of an electron-ion collision spectroscopy experiment setup	
	at a storage ring [Sch14]	10
2.8	Low-energy DR resonances of $F^{6+}$ as measured at the CRYRING	
	electron cooler in Stockholm. The red curve is a fit to the blue	
	experimental spectrum [BLS14]	11
2.9	Relative collision energy $E_{\rm col}$ in the CM frame in dependence of	
	the detuning voltage $U_{\rm det}$ in the laboratory for typical ion energies	
	of CRYRING [BLS14]	12
2.10	Procedure for energy scanning with detuning voltages and inter-	
	mediate cooling [BLS14]	13
3.1	Electric circuit diagram for an ohmic voltage divider	16
3.2	Equivalent circuit of the electrical design of the G35 divider (left)	
	and the low voltage part $R_{\rm LV}$ in detail (right). The corresponding	
	values are listed below [Win18b]	17
3.3	Photos of the upper part of the open G35 divider (left) and with	
	sealed vessel (right)	18
4.1	Electric circuit diagram of a simple mixed ohmic/capacitive voltage	
	divider	22
4.2	Schematic of the test setup	22
4.3	Electric circuit diagram of the test setup	23
4.4	Input signal (red) and output signal (blue) for a sine wave without	
	compensation $(C_{Var} = 0)$	24

4.5	Input signal (red) and output signal (blue) for a square pulse with- out compensation ( $C_{Var} = 0$ )	24
4.6	Input signal (red) and output signal (blue) for a sine wave with overcompensation ( $C_{Var} = 410 \text{ pF}$ )	25
4.7	Input signal (red) and output signal (blue) for a square pulse with overcompensation ( $C_{Var} = 410 \text{ pF}$ )	25
4.8	Input signal (red) and output signal (blue) for a sine wave with optimal compensation $(C_{Var} = (204 \pm 1) \text{ pF}).$	26
4.9	Input signal (red) and output signal (blue) for a square pulse with optimal compensation $(C_{Var} = (204 \pm 1) \text{ pF}).$	26
4.10	Input signal (red) and output signal (blue) for a square pulse with slight undercompensation $(C_{Var} = (202 \pm 1) \mathrm{pF})$	27
4.11	Input signal (red) and output signal (blue) for a square pulse with slight overcompensation $(C_{Var} = (206 \pm 1) \mathrm{pF})$	27
4.12	Measurements of a frequency compensated test setup with DC scale factor $M \approx 50$ [Dir17]	29
4.13	Equivalent electric circuit diagram of the G35 divider	30
4.14	Simulated response voltages of the compensated G35 divider ( $M=100.46:1$ ) to a 1 kV input pulse for varied capacitances $C_{\rm comp}$	31
4.15	Simulated response voltages of the compensated G35 divider ( $M = 100.46:1$ ) to a 1 kV input pulse for varied capacitances $C_{\text{comp}}$	31
4.16	Simulated response voltages of the compensated G35 divider ( $M = 100.46:1$ ) to a 1 kV input pulse for varied capacitances $C_{\rm HV}$	32
4.17	Simulated response voltages of the compensated G35 divider ( $M = 100.46:1$ ) to a 1 kV input pulse for varied capacitances $C_{\rm HV}$	32
5.1	Equivalent circuit diagram of the primary divider chain with $R_{\rm HV,1} = 20{\rm M}\Omega$ (left) and the low voltage part in detail (right) with $R_{\rm LV,1} = 2{\rm M}\Omega$ , $R_{\rm LV,2} = 1{\rm M}\Omega$ and $R_{\rm LV,3} = 100{\rm k}\Omega$	36
5.2	Equivalent circuit diagram of the fast divider	37
5.3	Equivalent circuit diagram of the frequency compensated divider.	39
5.4	Simulated response voltages of the compensated new fast divider $(M = 100:1)$ to a 1 kV input pulse for varied capacitances $C_{11}$ .	41
5.5	Simulated response voltages of the compensated new fast divider $(M = 100:1)$ to a 1 kV input pulse for varied capacitances $C_{HV}$ .	41
5.6	Preliminary 3D model of the new fast voltage divider. The low voltage side of the divider is continued in the box at the bottom.	43

5.7	Electric circuit diagram of $C_{\text{meas}}$ in detail, with switch $S_{\text{M}}$ to choose	
	the scale factor and switch $S_{\text{dev}}$ to choose the device	43