Fair Must Testing for I/O Automata

Rob van Glabbeek

University of Edinburgh, UK
University of New South Wales, Sydney, Australia

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The Theory of Testing [DH84]

Consider a model of concurrency that features *automata* and *tests*.
It does not matter how they are defined, provided the following:

- Each test has a set of *states*.
- Some states are *success states*.

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  Normally, automata are tests without success states.
  That is, tests are automata enriched with success states.

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A **must pass** T if each complete execution of $[T\|A]$ has a success state.
A **should pass** T [BRV95,NC95] if each finite execution of $[T\|A]$ can be extended into an execution with a success state.

$$A \equiv_{\text{should}} B \quad :\Leftrightarrow \quad \forall T.\ (A \textbf{ should pass } T \Leftrightarrow B \textbf{ should pass } T)$$

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Testing for CCS [DH84]

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states of a test: [. . .]
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Deadlock: a state without outgoing transitions

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Automata

An *automaton/test* A is $(\mathit{acts}(A), \mathit{states}(A), \mathit{start}(A), \mathit{steps}(A))$ with

- $\mathit{acts}(A)$ a set of *actions*,

- $\mathit{states}(A)$ a set of *states*,
- $\mathit{start}(A) \subseteq \mathit{states}(A)$ a nonempty set of *start states*, and
- $\mathit{steps}(A) \subseteq \mathit{states}(A) \times \mathit{acts}(A) \times \mathit{states}(A)$ a *transition relation*.

Automata are also known as *process graphs*,
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- $\mathit{acts}(A)$ a set of *actions*, partitioned into two sets $\mathit{ext}(A)$ and $\mathit{int}(A)$ of *external actions* and *internal actions*, respectively,
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sets of states in *labelled transition systems*.

An *execution* of an I/O automaton A is an alternating sequence $\alpha = s_0, a_1, s_1, a_2, \ldots$ of states and actions, either being infinite or ending with a state, such that $s_0 \in \mathit{start}(A)$ and $(s_i, a_{i+1}, s_{i+1}) \in \mathit{steps}(A)$ for all $i < \mathit{length}(\alpha)$.

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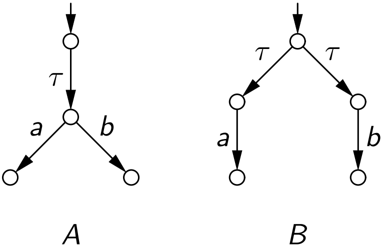
The theory of testing for CCS is a special case
of the theory of testing for automata.

Example: discerning branching time



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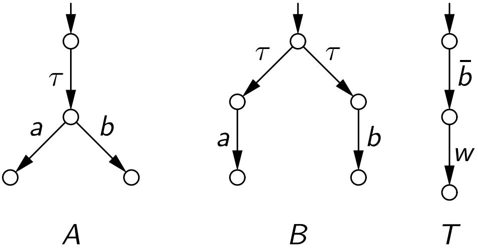

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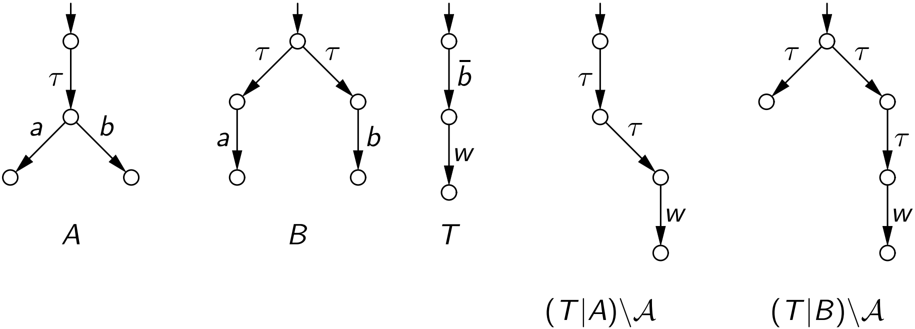

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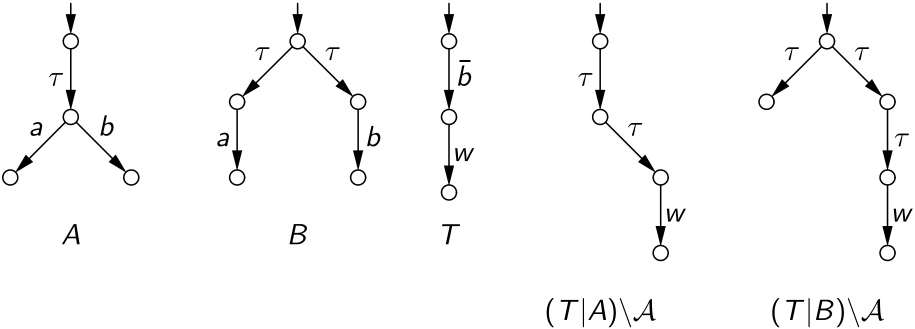

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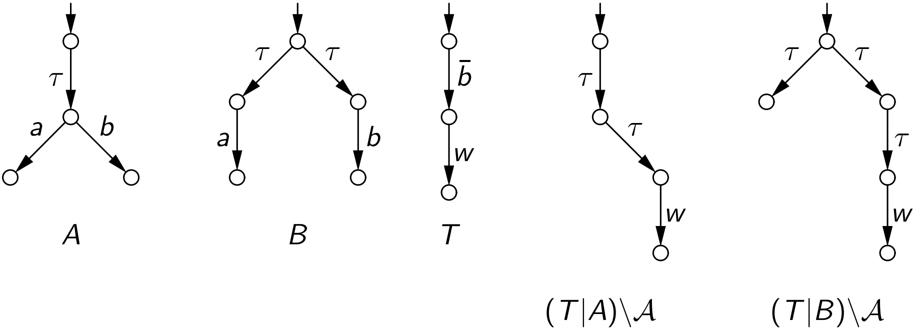

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This operator enforces synchronisation on $\mathit{ext}(T) \cap \mathit{ext}(A)$.

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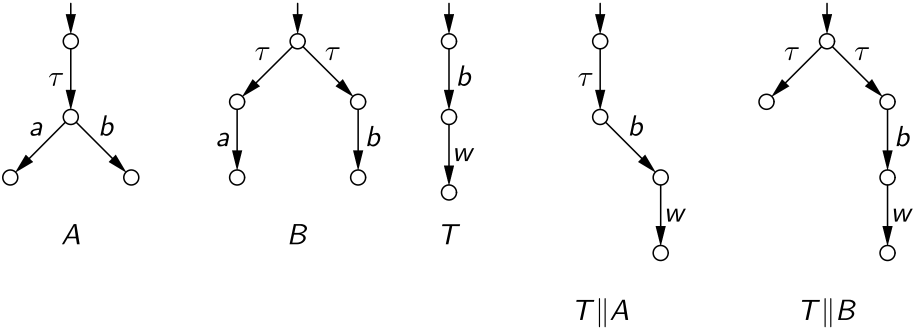

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I/O Automata [LT89]

Automata $A = (acts(A), states(A), start(A), steps(A) \qquad\qquad)$
in which

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- such that in each state each action from $in(A)$ is enabled,

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Automata $A = (\mathit{acts}(A), \mathit{states}(A), \mathit{start}(A), \mathit{steps}(A), \mathit{part}(A))$ in which

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An execution α of A is *fair* if, for each suffix α' of α
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Parallel composition $A \| B$ of I/O automata is as for CSP, or standard automata, but is defined only when $\mathit{out}(A) \cap \mathit{out}(B) = \emptyset$.

Fundamental Preorders on I/O Automata [LT89]

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$\mathit{trace}(\alpha)$ is the (in)finite sequence of external actions in execution α.
$\mathit{fintraces}(A) := \{\mathit{trace}(\alpha) \mid \alpha$ is a finite execution of $A\}$.
$\mathit{fairtraces}(A) := \{\mathit{trace}(\alpha) \mid \alpha$ is a fair execution of $A\}$.

$$S \sqsubseteq_T I \;:\Leftrightarrow\; \mathit{in}(S){=}\mathit{in}(I) \wedge \mathit{out}(S){=}\mathit{out}(I) \wedge \mathit{fintraces}(I) \subseteq \mathit{fintraces}(S)$$

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One writes $A \equiv_T B$ if $A \sqsubseteq_T B \wedge B \sqsubseteq_T A$, and similarly for $\equiv_F$.

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These preorders capture *safety* and *liveness* properties, respectively.

By [GH19, Thm. 6.1] each finite execution can be extended into a fair execution. As a consequence, $A \sqsubseteq_F B \Rightarrow A \sqsubseteq_T B$.

Testing for I/O Automata [Seg97]

automata: automata A with $w \notin \mathit{acts}(A)$
tests: automata T with $w \in \mathit{acts}(T)$
states of a test: $\mathit{states}(A)$
success states: those states in which w is enabled
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complete executions: either infinite, of ending in deadlock
application: the parallel composition $T \| A$

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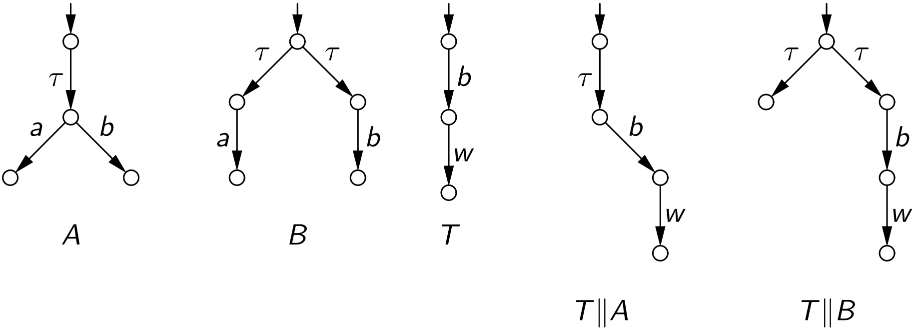
Example: discerning branching time impossible



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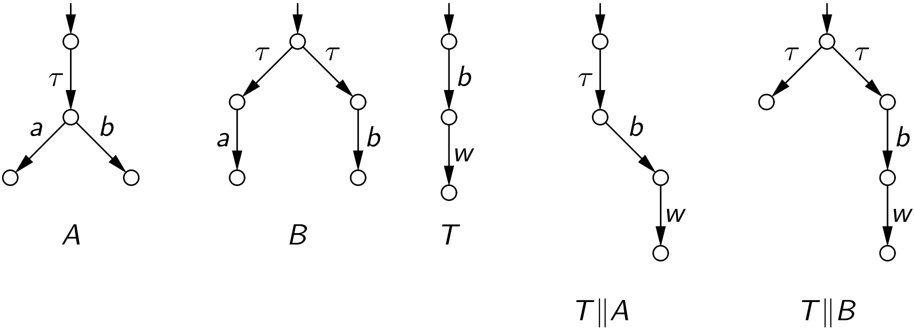
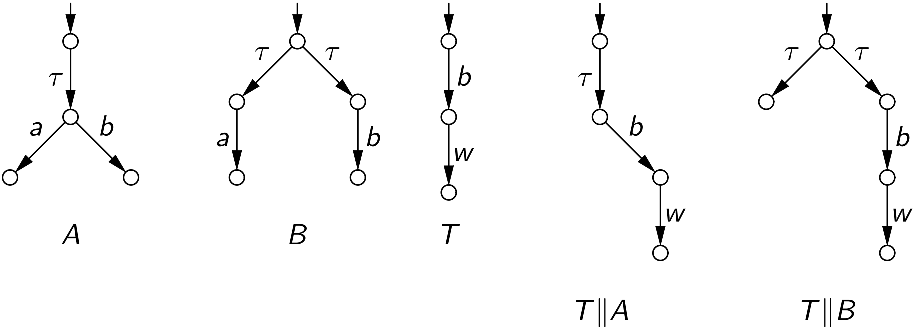


Such a T does not exists:

- if $a \notin ext(A)$ or $a \notin ext(T)$ then neither A nor B **must pass** T.
- $a \in in(A)$ or $a \in in(T)$ violates input enabledness
- if $a \in out(A) \cap out(T)$ then $T \| A$ is undefined.

Example: discerning branching time impossible



Such a T does not exists:

- if $a \notin$ *ext*(A) or $a \notin$ *ext*(T) then neither A nor B **must pass** T.
- $a \in$ *in*(A) or $a \in$ *in*(T) violates input enabledness
- if $a \in$ *out*$(A) \cap$ *out*(T) then $T \| A$ is undefined.

In fact, $A \equiv_{\text{must}} B$.

Safety and Liveness

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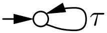
$A =$  $B =$  $\mathit{acts}(A) = \emptyset$ $\mathit{acts}(B) = \mathit{int}(B) = \{\tau\}$.

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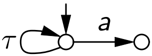
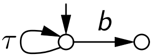


$\equiv_{must}$

$\not\equiv_F$



A Third Fundamental Preorder on I/O Automata [Va91]

$\mathit{trace}(\alpha)$ is the (in)finite sequence of external actions in execution α.
$\mathit{fintraces}(A) := \{\mathit{trace}(\alpha) \mid \alpha$ is a finite execution of $A\}$.
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$$S \sqsubseteq_T I \;:\Leftrightarrow\; \mathit{in}(S)=\mathit{in}(I) \wedge \mathit{out}(S)=\mathit{out}(I) \wedge \mathit{fintraces}(I) \subseteq \mathit{fintraces}(S)$$

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$$S \sqsubseteq_Q I :\Leftrightarrow S \sqsubseteq_T I \wedge qtraces(I) \subseteq qtraces(S)\,.$$

Theorem [Seg97]: Let A and B be finitely branching and strongly convergent I/O automata. Then $A \sqsubseteq_{\mathrm{must}} B$ iff $A \sqsubseteq_Q B$.

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In my analysis, this is because the classical theory of testing and I/O automata are based on different notions of a complete execution.

Testing for I/O Automata based on fairness

automata: I/O automata A with $w \notin \mathit{acts}(A)$
tests: I/O automata T with $w \in \mathit{out}(A)$
states of a test: $\mathit{states}(A)$
success states: those states in which w is enabled
executions: determined by $\mathit{steps}(A)$
complete executions: either infinite, of ending in deadlock
application: the I/O parallel composition $T \| A$

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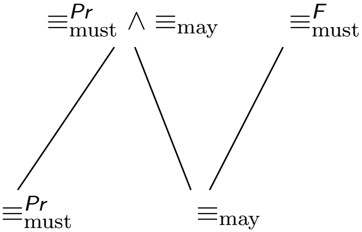
Theorem: Now $A \sqsubseteq_{\mathrm{must}} B$ iff $A \sqsubseteq_F B$.

A lattice of testing equivalences for I/O automata



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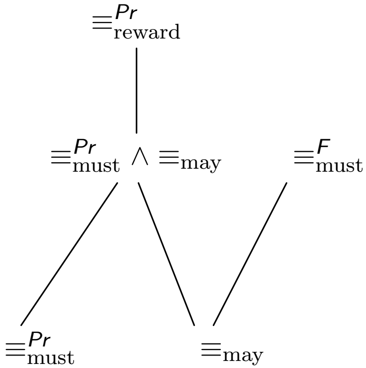

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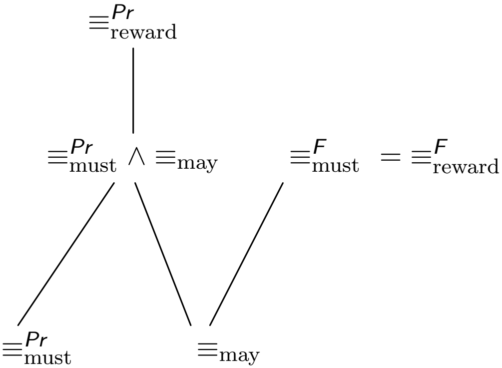
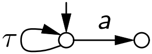
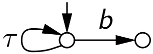


Counterexamples



$$\equiv^{Pr}_{\mathrm{must}}$$

$$\not\equiv_{\mathrm{may}}$$



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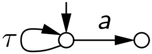

$$\not\equiv^{Pr}_{\mathrm{reward}}$$
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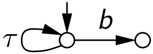

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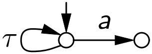

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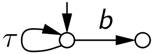

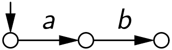

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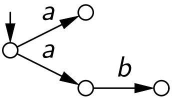

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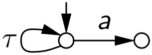

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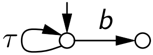

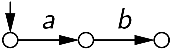

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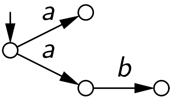

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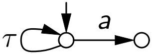

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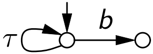

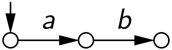

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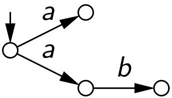

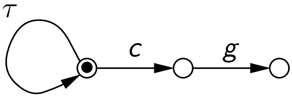

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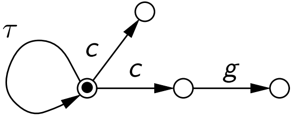

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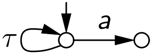

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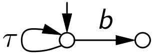

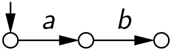

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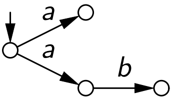

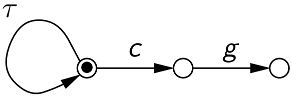

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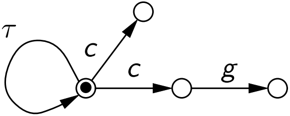

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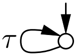
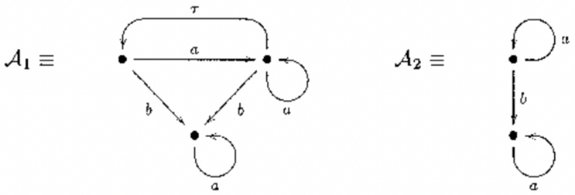


Counterexamples

EXAMPLE 5.2. Consider the I/O automata



where a is an input action, b is an output action, τ is an internal action, and the partitions of the locally controlled actions contain a single class. The I/O automata $\mathscr{A}_1$ and $\mathscr{A}_2$ are equivalent according to the quiescent preorder since they have the same external traces and their quiescent traces are all finite external traces containing at least a b action. The external trace a^∞, however, is a fair trace of $\mathscr{A}_1$ but not a fair trace of $\mathscr{A}_2$.

$\mathcal{A}_1 \equiv_{\text{reward}} \mathcal{A}_2$ but $\mathcal{A}_1 \not\equiv^F_{\text{must}} \mathcal{A}_2$.

$\mathcal{A}_1 \equiv_{\text{must}} \mathcal{A}_2$

$\mathcal{A}_1 \equiv_{\text{may}} \mathcal{A}_2$

Conclusion

When using the native notion of fairness from I/O automata as completeness criterion in the definition of must testing,

must testing exactly characterises the fair preorder from [LT89].

Upgrading to reward testing here does not yield extra distinctions.

Future work: extend with time and probabilities.