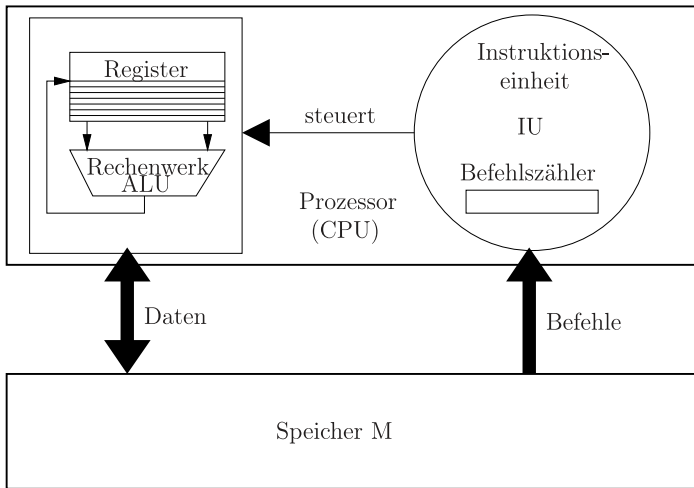
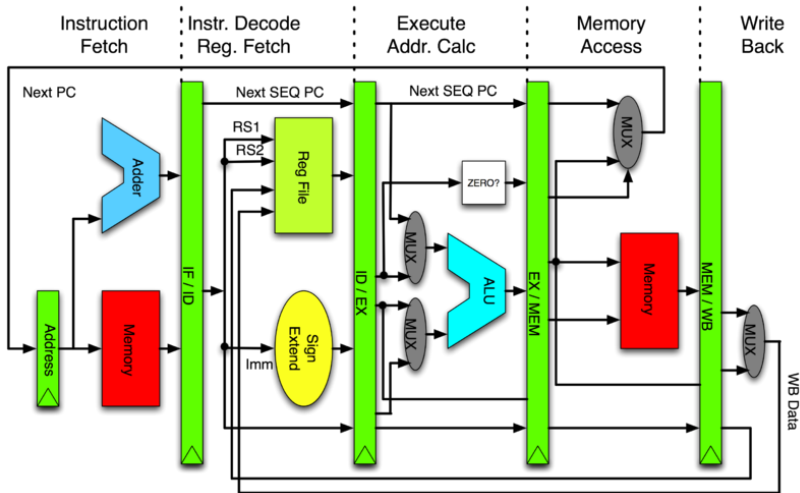


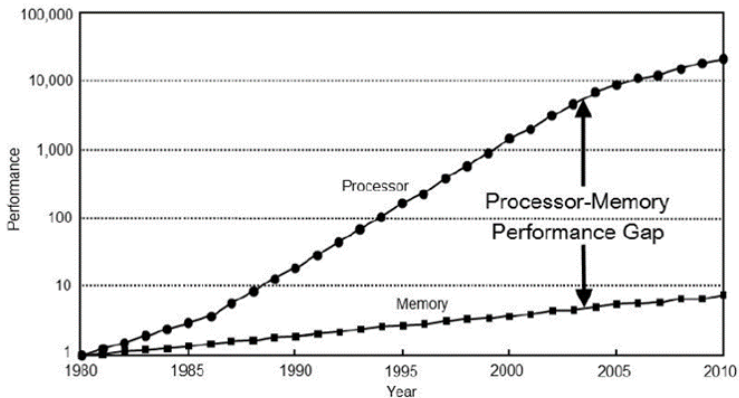
Von-Neumann Rechner



Aufbau des MIPS Prozessors

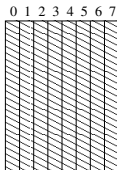


Memory gap

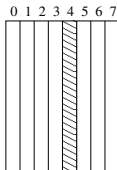


Einstufiger Cache – Platzierung

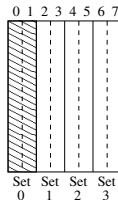
Voll assoziativ:
Block 12 kann in
jeden Cache-Block



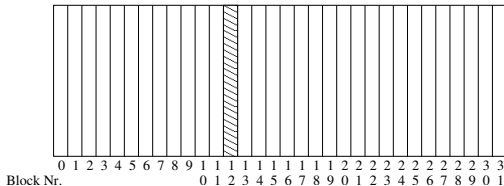
Direkte Zuordnung:
Block 12 kann nur in
Cache-Block 4
($12 \bmod 8$)



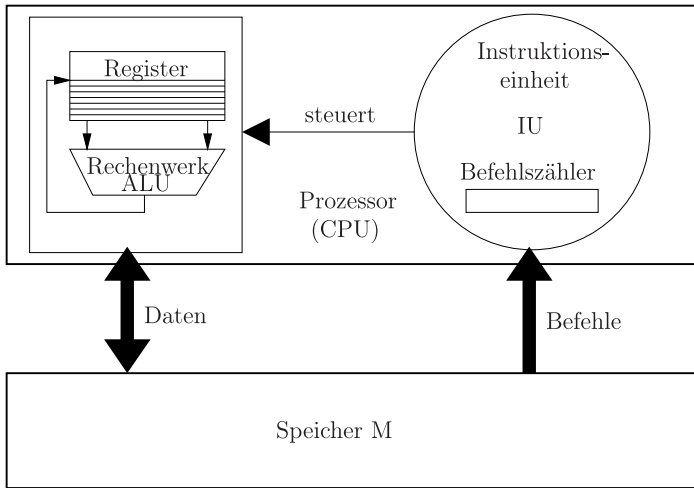
2-fach assoziativ:
Block 12 geht in
Menge 0 ($12 \bmod 4$)



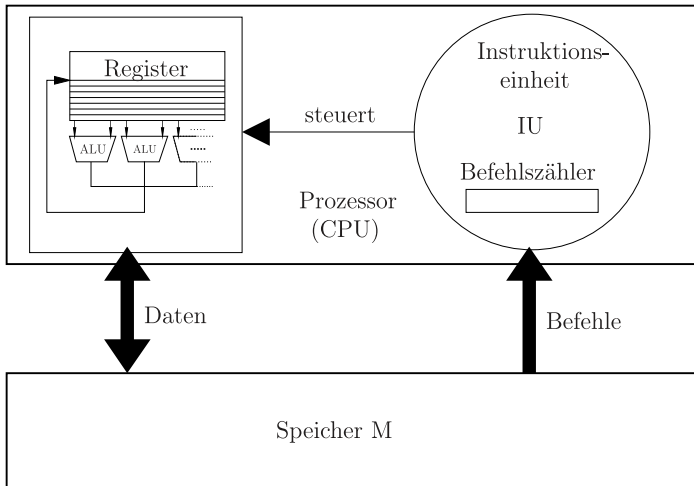
Hauptspeicher:



SIMD Prozessor

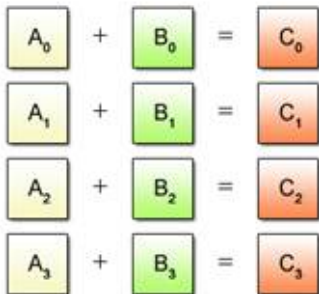


SIMD Prozessor

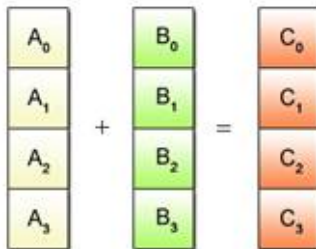


Vektorisierung Konzept

(a) Scalar Operation



(b) SIMD Operation



Bilder: <https://www.kernel.org/>, Cell Programming Tutorial

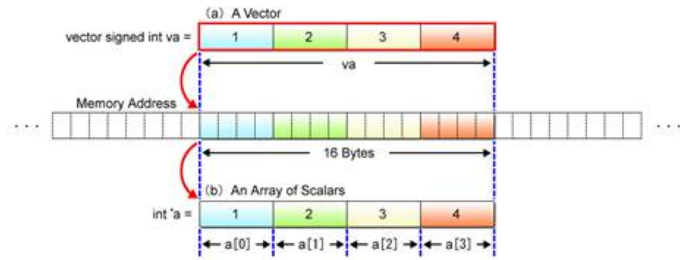
Vektorisierung Konzept

Nicht möglich!

$$\begin{array}{r} A_0 + B_0 = C_0 \\ A_1 - B_1 = C_1 \\ A_2 \times B_2 = C_2 \\ A_3 \div B_3 = C_3 \end{array}$$

Bilder: <https://www.kernel.org/>, Cell Programming Tutorial

Vektorisierung Konzept



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- ▶ MPI-parallel, Multi-core, SIMD
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- ▶ Beworbene Peak Performance: 486.4 GFlop/s

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 - ▶ $4 \times$ SIMD → ohne AVX: 3.8 GFlop/s
- klassischer, nicht-paralleler Code begrenzt auf 3.8 GFlop/s
- man verliert 99% der Leistung